8 D/A and A/D Converter

Syllabus

Introduction, Basic DAC techniques, Weighted resistor DAC, R - 2R ladder DAC, Inverted R - 2R DAC, and IC 1408 DAC, Different types of ADCs - Parallel comparator type ADC, Counter type ADC, Successive approximation ADC and dual slope ADC, DAC and ADC specifications, Specifications AD 574 (12 bit ADC).

Contents

8.1 Introduction

Most of the information carrying signals such as voltage, current, charge, temperature, pressure and time are available in the analog form. However, for processing, transmission and storage purposes, it is often more convenient to express such signals in the digital form. When expressed in the digital form, they provide better accuracy and reduce noise.

Moreover, the development in the microprocessor technology has made it compulsory to process data in the digital form. Since digital systems such as microprocessor use a binary system of ones and zeros, we have to convert signal from analog form to digital form. The circuit that performs this conversion is called an analog to digital (A/D) converter.

On the other hand, a digital to analog (D/A) converter is used when a binary output from a digital system must be converted to some equivalent analog voltage or current. For example, if in a particular system a computer is used as a controller, the controlling signal produced by the computer is always digital. The system to be controlled requires the analog signal. Hence in between the computer and the system to be controlled the digital to analog converter is must.

Fig. 8.1 shows a typical A/D and D/A converter application. As shown in the Fig. 8.1, the analog signal is converted in digital form, which is then processed or perhaps just transmitted or recorded. Once processed, received, or retrieved, the signal is D-A converted to be reused in analog form.

In this chapter, we see the various techniques used for analog to digital conversion and digital to analog conversion.

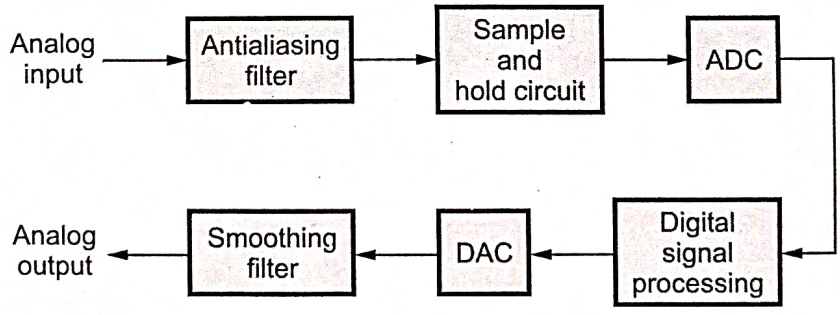

Fig. 8.1 Typical A/D and D/A converter application

8.2 D/A Converters

Dec.-11, Set-3

A DAC (Digital to Analog Converter) accepts an n-bit input word b_1, b_2, b_3, ... b_n in binary and produce an analog signal proportional to it. Fig. 8.2 shows circuit symbol and input-output characteristics of a 4-bit DAC. There are four digital inputs, indicating 4-bit DAC. Each digital input requires an electrical signal representing either a logic 1 or

logic 0. The b_n is the least significant bit, LSB, whereas b_1 is the most significant bit, MSB.

Fig. 8.2 (b) shows analog output voltage V_o is plotted against all 16 possible digital input words.

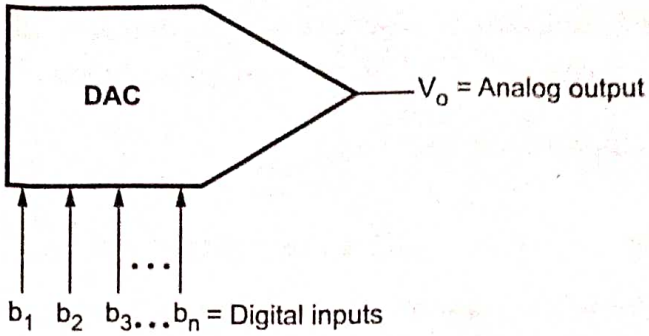

Fig. 8.2 (a) DAC circuit symbol

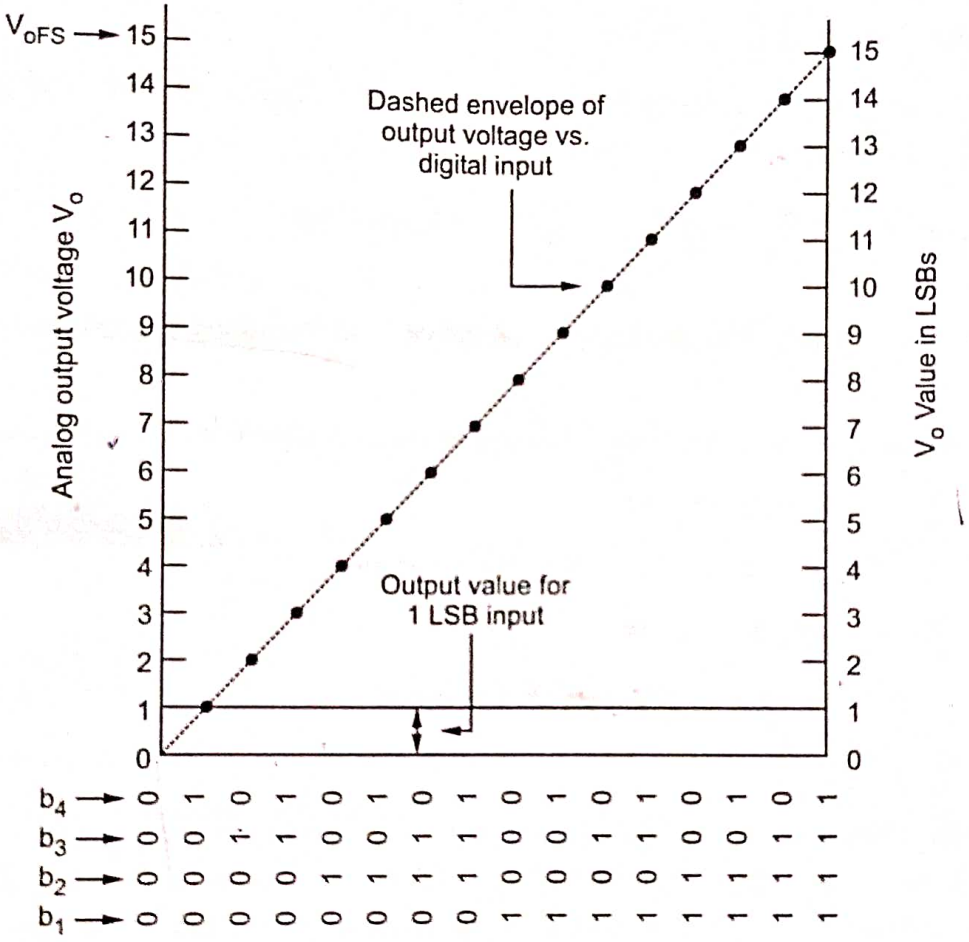

Fig. 8.2 (b)

8.2.1 Performance Parameters Specifications of DAC

The various performance parameters of DAC are,

Resolution

Resolution is defined in two ways.

- Resolution is the number of different analog output values that can be provided by a DAC. For an n-bit DAC

Resolution = 2^n ... (1)

- Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs. For an n-bit DAC it can be given as

$$\text{Resolution} = \frac{V_{oFS}}{2^n - 1} \quad \ldots (2)$$

where, V_{oFS} = Full scale output voltage

From equation 1, we can say that, the resolution can be determined by the number of bits in the input binary word. For an 8-bit DAC resolution can be given as

$$\text{Resolution} = 2^n = 2^8 = 256$$

If the full scale output voltage is 10.2 V then by second definition the resolution for an 8-bit DAC can be given as

$$\text{Resolution} = \frac{V_{oFS}}{2^n - 1} = \frac{10.2}{2^8 - 1} = \frac{10.2}{255} = 40 \text{ mV/LSB}$$

Therefore, we can say that an input change of 1 LSB causes the output to change by 40 mV.

From the resolution, we can obtain the input-output equation for a DAC.

Thus V_o = Resolution × D

where D = Decimal value of the digital input

and V_o = Output voltage

The resolution takes care of changes in the input.

Accuracy

It is a comparison of actual output voltage with expected output. It is expressed in percentage. Ideally, the accuracy of DAC should be, at worst, ± ½ of its LSB. If the full scale output voltage is 10.2 V then for an 8-bit DAC accuracy can be given as

$$\text{Accuracy} = \frac{V_{oFS}}{(2^n - 1)\,2} \quad \ldots (3)$$

$$= \frac{10.2}{255 \times 2} = 20 \text{ mV}$$

Settling Time (Conversion Time)

The operating conversion speed of a DAC is usually specified by giving its settling time. The settling time is the time required for the DAC output to 90 form zero to full scale as the binary input is changed from all 0s to all 1s. Actually, the settling time is

measured as the time for the DAC output to settle within ±1/2 step size (1/2 LSB) of its final value.

Typical values for settling time range from 50 ns to 10 μs. It depends on word length, circuit technology and architecture. Generally, DAC's with a current output will have shorter settling times than those with voltage outputs.

Dynamic Range

The dynamic range of DAC is defined as the ratio of the largest output to the smallest output, excluding zero. It is expressed in dB. For linear DACs it is given by,

$$\text{Dynamic range} = 20 \log 2^n \approx 6n.$$

For companding type DAC, the dynamic range is more. It is typically 66 to 72 dB.

Offset Error

The offset error is defined as the nonzero level of the output voltage when all inputs are zero.

It adds a constant value to all output values, as shown in Fig. 8.3.

It is due to the presence of offset voltage in op-amp and leakage currents in the current switches.

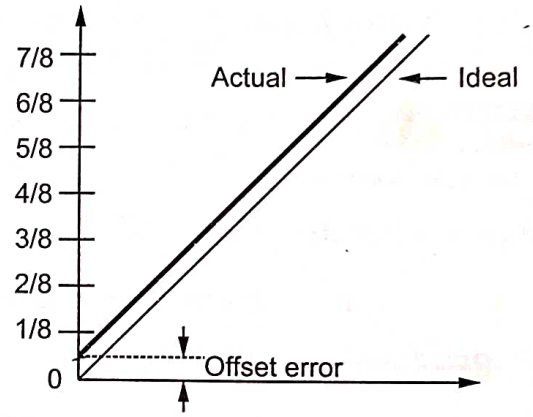

Fig. 8.3 Offset error in transfer characteristics of DAC

Gain Error

The gain error is defined as the difference between the calculated gain of the current to voltage converter and the actual gain achieved. It is due to the errors in the feedback resistor on the current to voltage converter op-amp.

Fig. 8.4 shows the gain error in transfer characteristics of DAC.

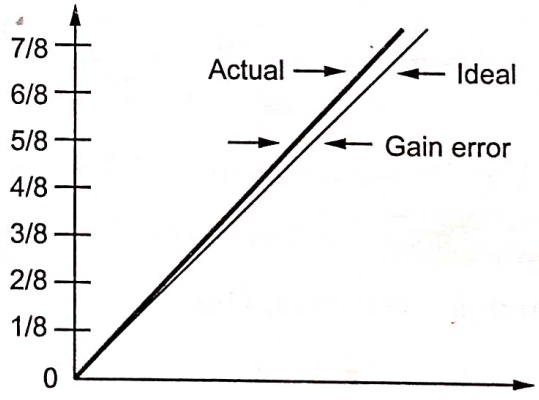

Fig. 8.4 Gain error in transfer characteristics of DAC

Non-Linearity (Linearity Error)

An ideal DAC should be linear. For an ideal DAC, the output voltage would be a linear function of the input code. But it is fact that all DAC departs somewhat from the ideal linearity. The typical factors responsible for introducing non-linearity are :

- Non-exact value of resistors, and
- Non-ideal electronic switches that introduce extra resistance to the circuit.

The non-linearity error is the amount by which the actual output differs from the ideal straight-line output. The different types of non-linearity are :

- Integral non-linearity,
- Differential non-linearity.

Stability

The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges. These parameters represent the stability of the converter.

Monotonicity

A converter is said to have good monotonicity if it does not miss any step backward when stepped through its entire range by a counter.

8.2.2 Basic DAC Techniques

There are mainly two techniques used for analog to digital conversion,

- Binary weighted resistor D/A converter
- R/2R ladder D/A converter

In these techniques, the shunt resistors are used to generate n binary weighted currents. These currents are added according to switch positions controlled by the digital input and then converted into voltage to give analog voltage equivalent to the digital input. Therefore, such digital to analog converters are called **current driven DACs.**

8.2.2.1 Binary Weighted Resistor D/A Converter

The binary weighted resistor DAC uses an op-amp to sum n binary weighted currents derived from a reference voltage V_R via current scaling resistors 2R, 4R, 8R, ..., 2^n R, as shown in the Fig. 8.5.

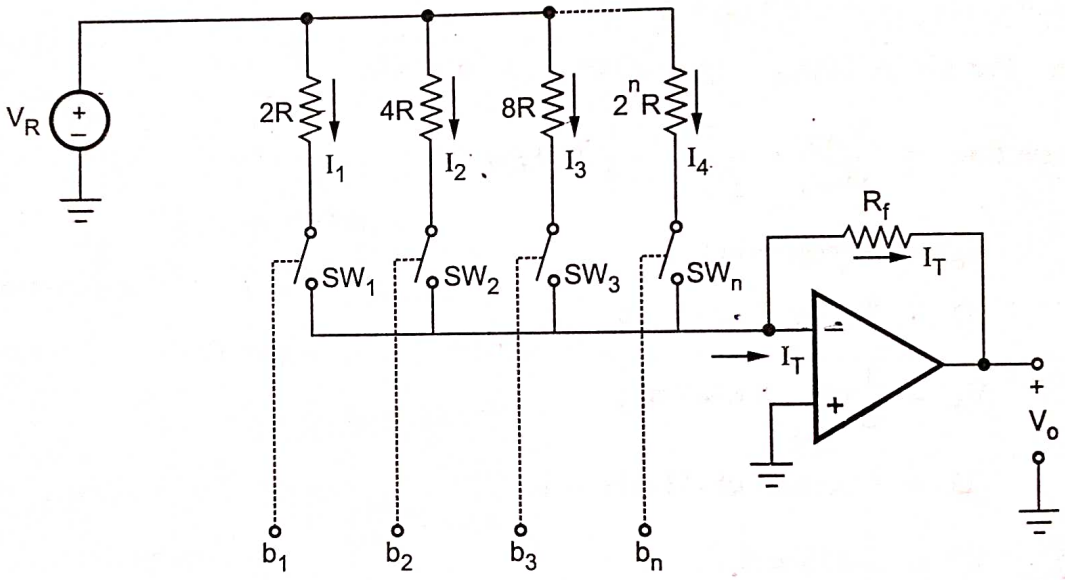

Fig. 8.5 Binary weighted resistor DAC

As shown in the Fig. 8.5, switch positions are controlled by the digital inputs. When digital input is logic 1, it connects the corresponding resistance to the reference voltage V_R; otherwise it leaves resistor open. Therefore,

For ON-switch, $I = \frac{V_R}{R}$ and

For OFF-switch, $I = 0$

Here, operational amplifier is used as a summing amplifier. Due to high input impedance of op-amp, summing current will flow through R_f. Hence the total current through R_f can be given as

$$I_T = I_1 + I_2 + I_3 + \cdots + I_n$$

The output voltage is the voltage across R_f and it is given as

$$V_o = -I_T R_f = -(I_1 + I_2 + I_3 + \cdots + I_n) R_f$$

$$= -\left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \cdots + b_n \frac{V_R}{2^n R} \right) R_f$$

$$= -\frac{V_R}{R} R_f \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right) \quad \ldots (4)$$

When $R_f = R$, V_o is given as

$$V_o = -V_R \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right) \quad \ldots (5)$$

The equation (4) indicates that the analog output voltage is proportional to the input digital word.

The simplicity of the binary weighted DAC is offset by drawbacks associated with it.

Drawbacks :

1. Wide range of resistor values are required. For 8-bit DAC, the resistors required are 2^1 R, 2^2 R, 2^3 R, ... and 2^8 R. Therefore, the largest resistor is 128 times the smallest one.
2. This wide range of resistor values has restrictions on both, higher and lower ends. It is impracticable to fabricate large values of resistor in IC, and voltage drop across such a large resistor due to the bias current also affects the accuracy. For smaller values of resistors, the loading effect may occur.
3. The finite resistance of the switches disturbs the binary-weighted relationship among the various currents, particularly in the most significant bit positions, where the current setting resistances are smaller.

All these drawbacks, especially the requirement of wide range of resistors restricts the use of binary weighted resistor DACs below 8-bits.

8.2.2.2 Inverted R / 2R Ladder (Current Steering Mode) D/A Converter

R/2R ladder D/A converter uses only two resistor values. This avoids resistance spread drawback of binary weighted D/A converter. Fig. 8.6 shows R/2R ladder DAC. Like binary weighted resistor DAC, it also uses shunt resistors to generate n binary weighted currents; however it uses voltage scaling and identical resistors instead of resistor scaling and common voltage reference used in binary weighted resistor DAC. Voltage scaling requires an additional set of voltage dropping series resistances between adjacent nodes, as shown in the Fig. 8.6.

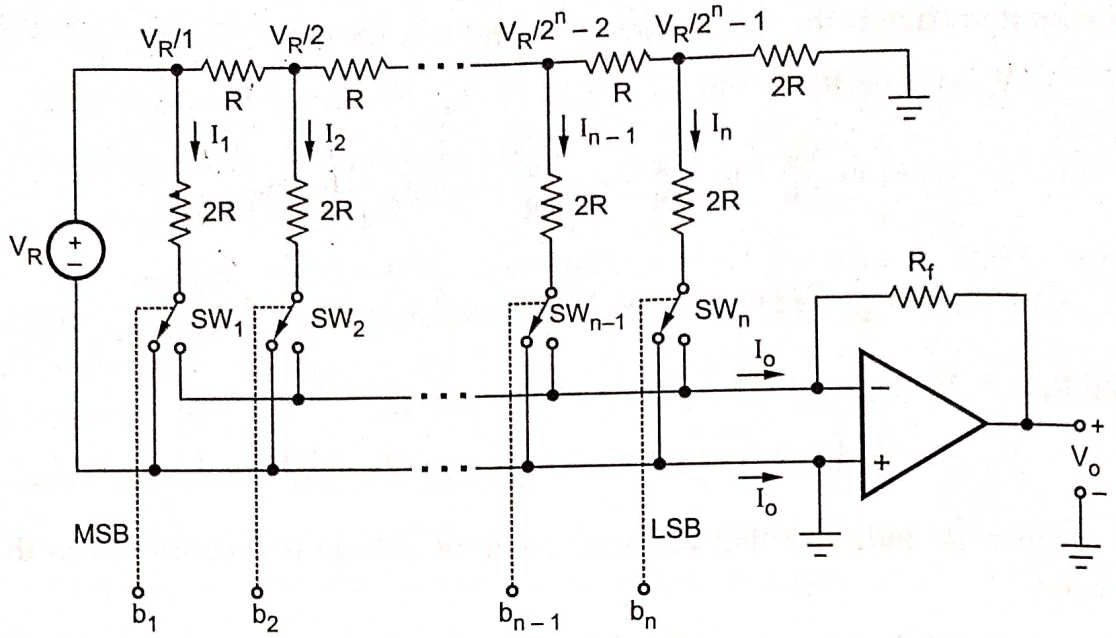

Fig. 8.6

Here, each bit of the binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is at the virtual ground. Since both the positions of switches are at ground potential, the current flowing through resistances is constant and it is independent of switch position. These currents can be given as,

$$I_1 = \frac{V_R}{2R} \quad \ldots (6)$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

$$I_n = \frac{V_R/2^n - 1}{2R} = \frac{I_1}{2^n - 1} \quad \ldots (7)$$

We know that, V_o is given as,

$$V_o = -I_T R_f \quad \ldots (8)$$

$$V_o = -R_f (I_1 + I_2 + I_3 + \cdots + I_n)$$

$$= -R_f \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \cdots + b_n \frac{V_R}{2^n R} \right)$$

$$= \frac{-V_R R_f}{R} \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right) \quad \ldots (9)$$

When $R_f = R$, V_o is given as,

$$V_o = -V_R \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n}\right) \quad \ldots (10)$$

Let us consider 4-bit binary DAC with binary input 1001 and $R_f = R$, as shown in the Fig. 8.7.

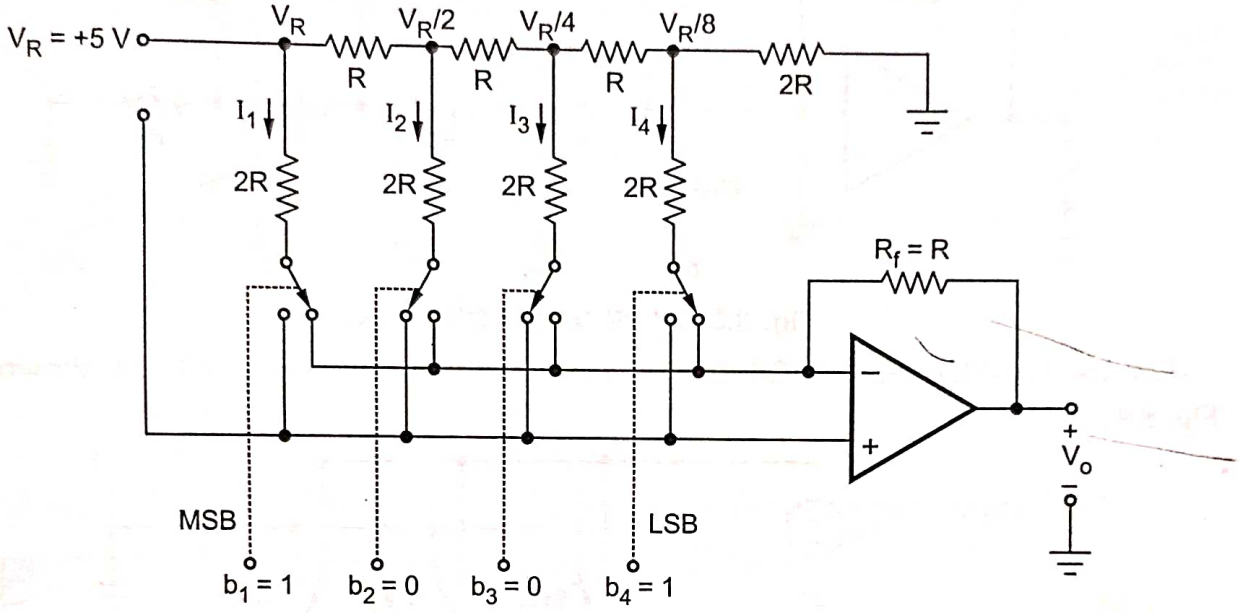

Fig. 8.7 Inverted 4-bit R / 2R ladder DAC

Here, output voltage is given as

$$V_o = -V_R (1\times 2^{-1} + 0\times 2^{-2} + 0\times 2^{-3} + 1\times 2^{-4})$$

$$= -V_R \left(\frac{1}{2} + 0 + 0 + \frac{1}{16}\right) = -0.5625\ V_R = 2.8125\ V$$

The inverting R/2R ladder DAC works on the principle of summing currents and it is also said to operate in the **current steering mode**. An important advantage of the current mode is that all ladder node voltages remain constant with changing input codes, thus avoiding any shutdown effects by stray capacitances.

8.2.2.3 R / 2R Ladder (Voltage Switching Mode) D/A Converter

In this type, reference voltage is applied to one of the switch positions, and other switch position is connected to ground, as shown in the Fig. 8.8.

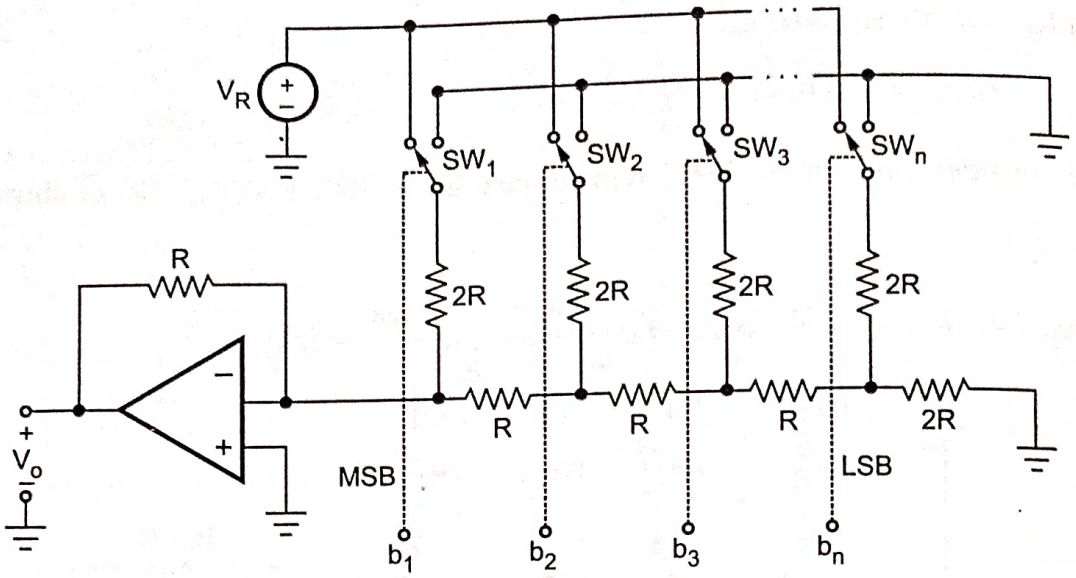

Fig. 8.8 R / 2R ladder D/A converter

Let us consider 3-bit R/2R ladder DAC with binary input 001, as shown in the Fig. 8.9.

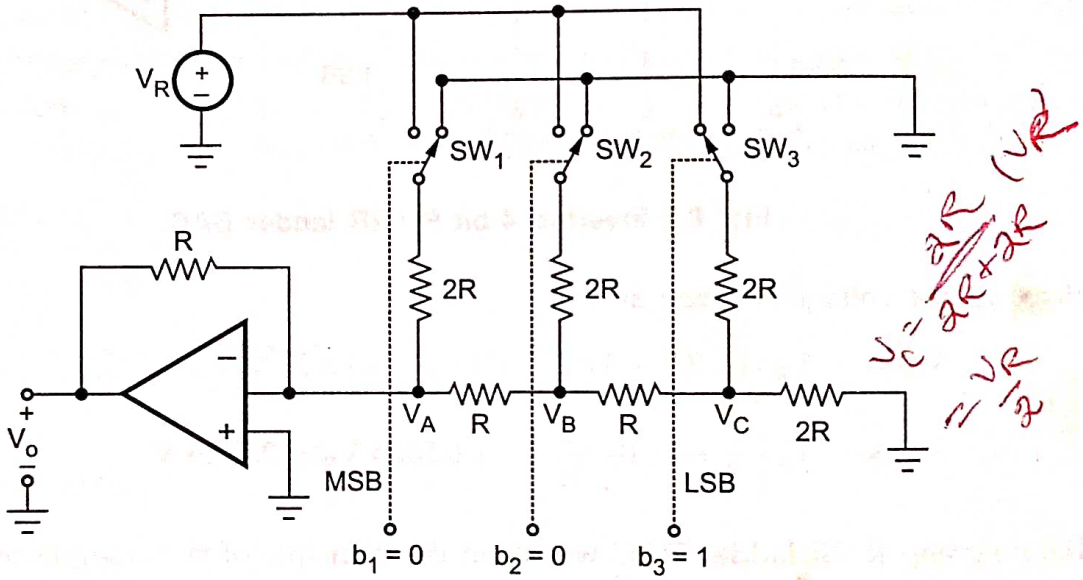

Fig. 8.9 3-bit R / 2R ladder DAC

Reducing above network to the left by Thevenin's theorem we get,

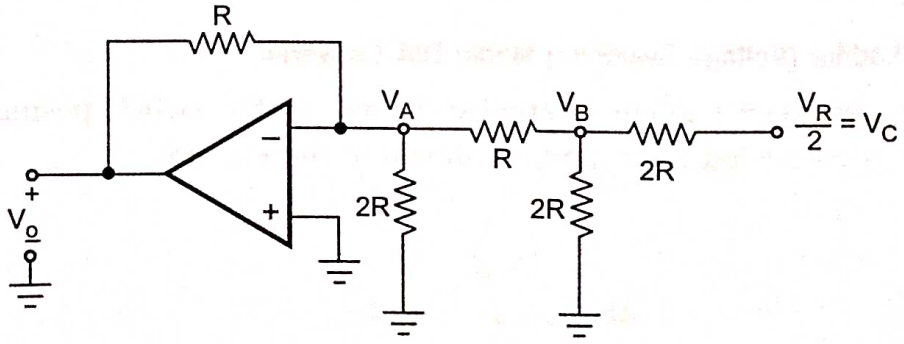

Fig. 8.10 (a)

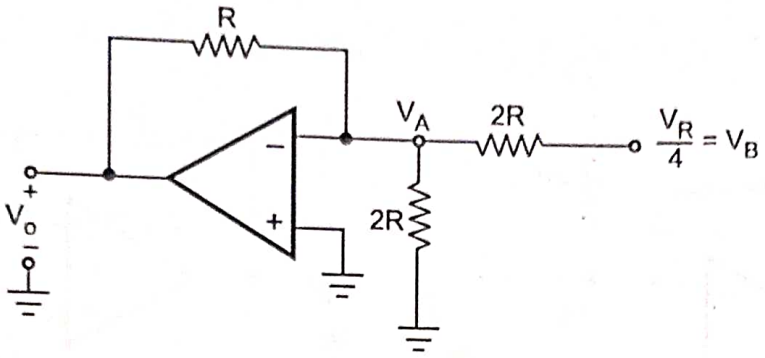

Fig. 8.10 (b)

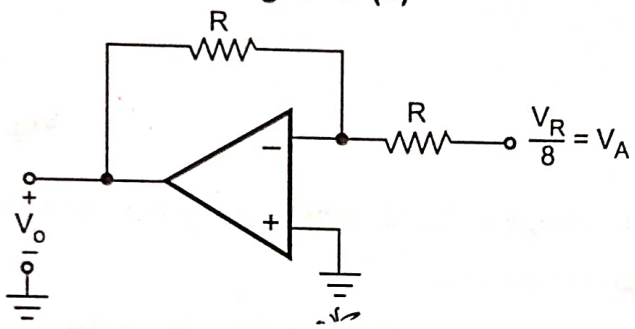

Fig. 8.10 (c)

Therefore, the output voltage is $V_R/8$ which is equivalent to binary input 001.

For binary input 100 the network can be reduced as follows :

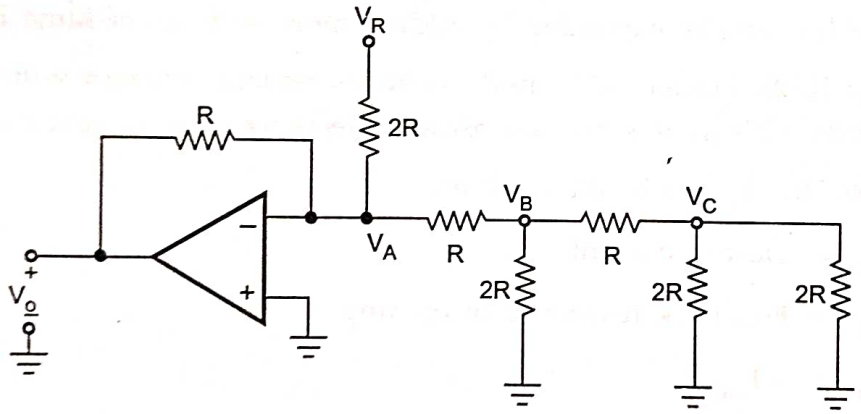

Fig. 8.11 (a)

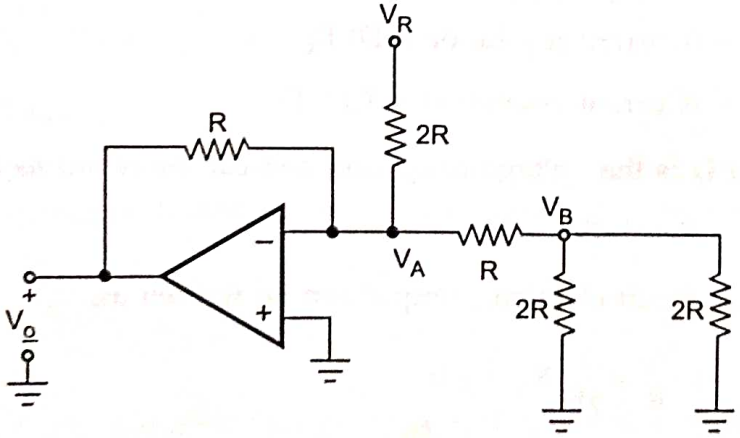

Fig. 8.11 (b)

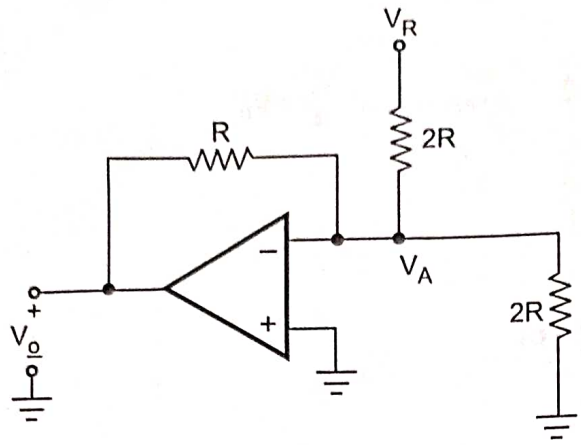

Fig. 8.11 (c)

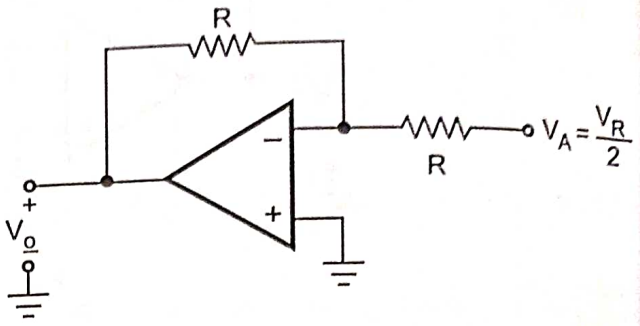

Fig. 8.11 (d)

Therefore, the output voltage is $V_R/2$, which is equivalent to binary input 100.

In general, the voltage is given by

$$V_o = - V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + ... + b_n 2^{-n})$$

Advantages of R/2R ladder DACs

1. Easier to build accurately as only two precision metal film resistors are required.
2. Number of bits can be expanded by adding more sections of same R/2R values.
3. In inverted R/2R ladder DAC, node voltages remain constant with changing input binary words. This avoids any slowdown effects by stray capacitances.

The expression for V_o can be obtained as,

Let I_{out} = Output current

R_f = Feedback resistance of op-amp

$\therefore$ $V_o = - I_{out} R_f$

Now I_{out} = Current resolution × D

$\therefore$ V_o = – (Current resolution × D) R_f

$\therefore$ V_o = – (Current resolution × R_f) × D ... (11)

The coefficient of D is the voltage resolution and can be called as simple resolution.

$\therefore$ V_o = – Resolution × D ... (12)

In terms of actual circuit elements, output can be written as,

$$V_o = -\left(\frac{V_R}{R} \times \frac{1}{2^n} R_f \right) \times D \quad ...(13)$$

The resolution of R/2R ladder type DAC with current output is,

$$\text{Resolution} = \frac{1}{2^n} \times \frac{V_R}{R} \quad \ldots (14)$$

while the resolution fo R/2R ladder type DAC with voltage output is,

$$\text{Resolution} = \left(\frac{1}{2^n} \times \frac{V_R}{R} \right) \times R_f \quad \ldots (15)$$

Example 8.6 *Suggest the values of resistors and reference voltage if resolution required is 0.5 V for 4 bit R/2R ladder type DAC.*

Solution : Resolution $= \left(\frac{1}{2^n} \times \frac{V_R}{R} \right) \times R_f$

Let $V_R = 10$ V, n = 4 and resolution = 0.5

$\therefore \quad 0.5 = \frac{1}{2^4} \times \frac{10}{R} \times R_f$

$\therefore \quad \frac{R}{R_f} = 1.25$

Choose $R_f = 10\ k\Omega$

$\therefore \quad R = 12.5\ k\Omega$

Example 8.7 *Calculate the number of bits required to represent a full scale voltage of 10 V with a resolution of 5 mV approximately.* **Dec.-11, Set-3, Marks 5**

Solution : Resolution $= \frac{V_{OFS}}{2^n - 1}$

$\therefore \quad 2^n = \frac{V_{OFS}}{\text{Resolution}} + 1 = \frac{10}{5\ mV} + 1 = 2001$

When n = 11 we have $2^n = 2048$. Therefore, minimum 11 bits are required to represent a full scale voltage of 10 V.

8.2.2.4 Multiplying DACs

A digital to analog converter which uses a varying reference voltage is called a **multiplying D/A converter (MDAC)**. We know that, the output voltage for DAC is given by,

$$V_o = -\frac{V_R}{R} R_f (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_n 2^{-n})$$

In this equation, if the reference voltage V_R is applied as sine wave given by

$$V_R(t) = V_{im} \cos 2\pi ft$$

Then $V_o(t) = V_{om} \cos (2\pi ft + 180°)$ and V_{om} will vary from 0 V to $(1 - 2^{-n})\ V_{im}$ depending upon the input digital code.

The output of MDAC is a fraction of the voltage representing the input digital code. Thus the MDAC can be used as digitally controlled audio attenuator where attenuator setting are controlled by digital code.

The MDAC with op-amp as an integrator connected at the output of it provides digitally programmable integration. Such an integration can be used in the design of digitally programmable oscillators and filters.

8.2.2.5 Current Driven DAC

In R/2R ladder type DAC we can expand the resolution of DAC by adding more ladders. We know that, the current through first ladder is $\frac{V_R}{2R}$, second ladder is $\frac{V_R}{4R}$, third ladder is $\frac{V_R}{8R}$ and so on. When switches of such ladders are realized with BJTs, the emitter current of each BJT is current through corresponding ladder. Therefore, they are not equal. They are multiples of 2^n. When such DAC are fabricated using monolithic technology, it is necessary to maintain ratioed emitter area to pass ratioed emitter current. This leads to extravagant transistor geometries. This problem of ratioed emitter area can be eliminated altogether by using equal-value current sinks and exploitting the current-scaling capability of the inverted R-2R ladder to obtain binary-weighted contributions to the output. Such DACs are known as **current driven DACs.**

The Fig. 8.12 shows 4-bit current driven DAC. For the 4-bit current driven DAC shown in Fig. 8.12, the current I_o is given by

$$I_o = 2\frac{V_r}{R_r}\left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + b_4 2^{-4}\right)$$

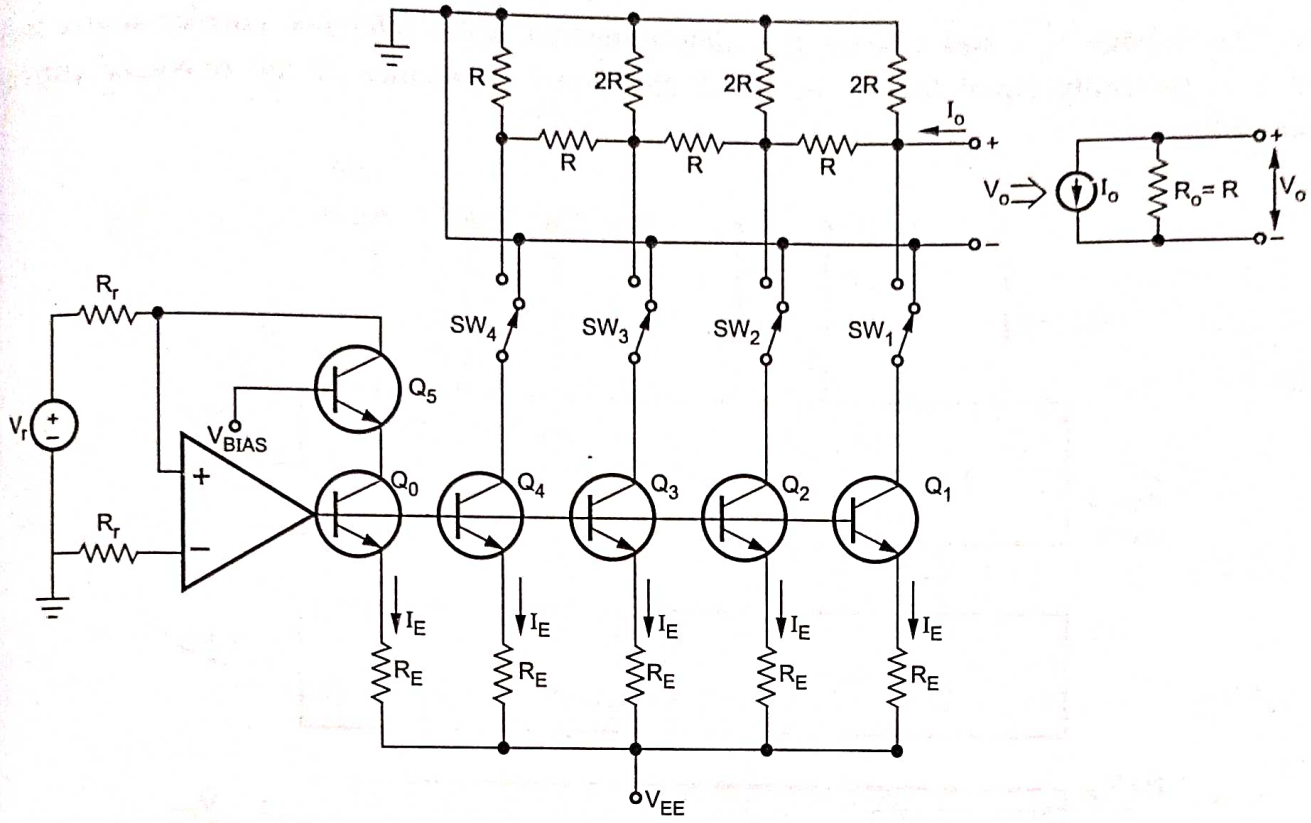

Fig. 8.12 4-bit current driven DAC

8.3 IC 1408 DAC

The 1408, is an 8 bit R/2R ladder type D/A converter compatible with TTL and CMOS logic. It is designed to use where the output current is linear product of an eight bit digital word.

Fig. 8.13 (a) shows the pin diagram and block diagram for IC 1408 DAC.

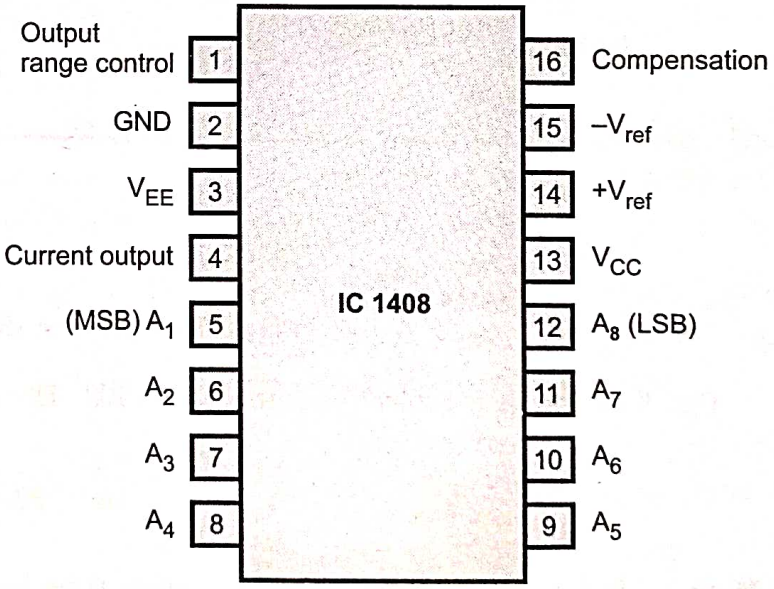

Fig. 8.13 (a) Pin diagram

The IC 1408 consists of a reference current amplifier, an R/2R ladder and eight high speed current switches. It has eight input data lines A_1 (MSB) through A_8 (LSB) which control the positions of current switches.

It requires 2 mA reference current for full scale input and two power supplies V_{CC} = + 5 V and V_{EE} = – 15 V (V_{EE} can range from – 5 V to – 15 V).

The voltage V_{ref} and resistor R_{14} determines the total reference current source and R_{15} is generally equal to R_{14} to match the input impedance of the reference current amplifier.

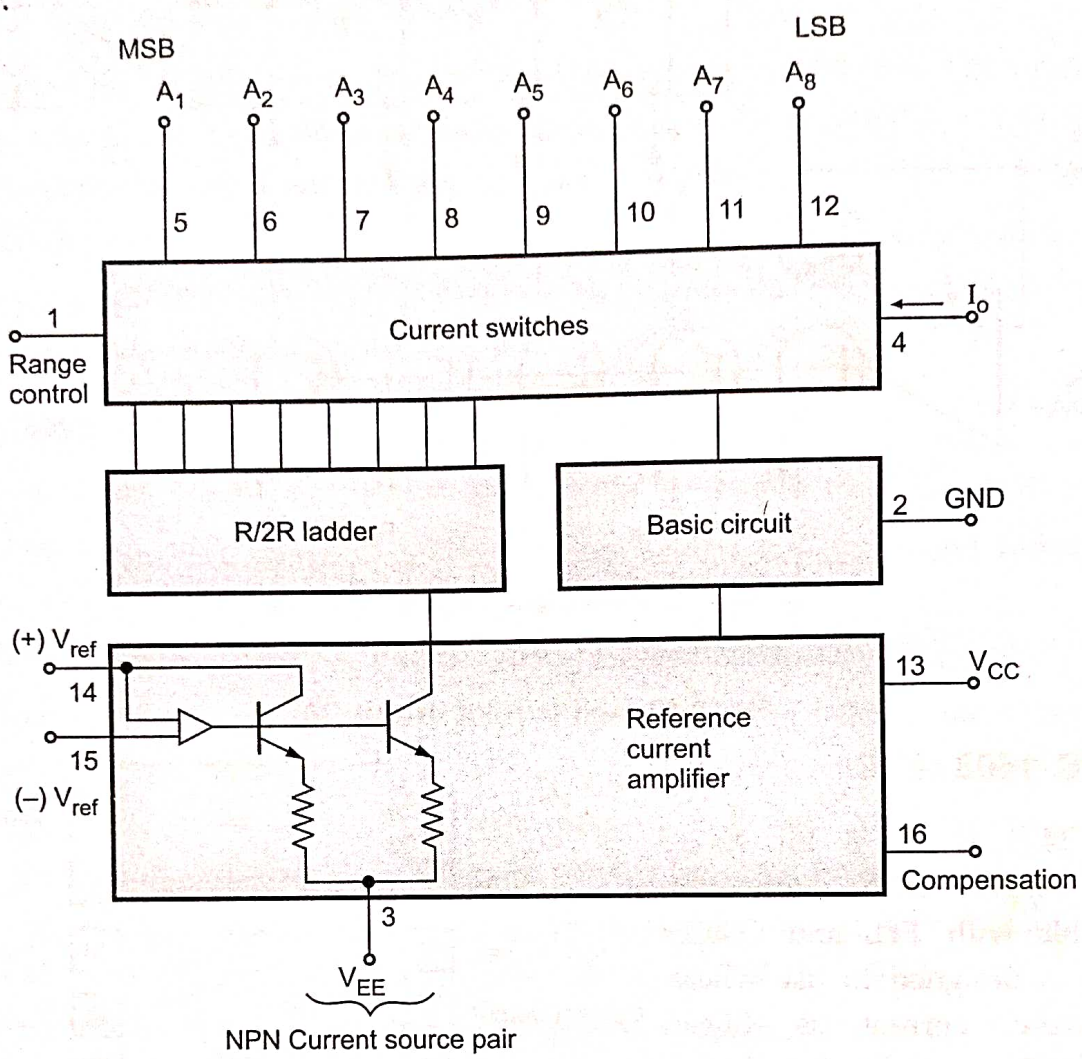

Fig. 8.13 (b) Block diagram

Fig. 8.14 shows a typical circuit for IC 1408. The output current I_o can be given as

$$I_o = \frac{V_{ref}}{R_{14}}\left(\frac{A_1}{2}+\frac{A_2}{4}+\frac{A_3}{8}+\frac{A_4}{16}+\frac{A_5}{32}+\frac{A_6}{64}+\frac{A_7}{128}+\frac{A_8}{256}\right) \quad ...(1)$$

Note : Input A_1 through A_8 can be either 0 or 1. Therefore, for typical circuit full scale current can be given as,

$$I_o = \frac{5}{2.5\,K}\left(\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right) = \frac{2\,mA \times 255}{256} = 1.992\ mA$$

It shows that the full scale output current is always 1 LSB less than the reference current source of 2 mA. This output current is converted into voltage by I to V converter. The output voltage for full scale input can be given as

$$V_o = 1.992 \times 2.5\ K = 4.98\ V$$

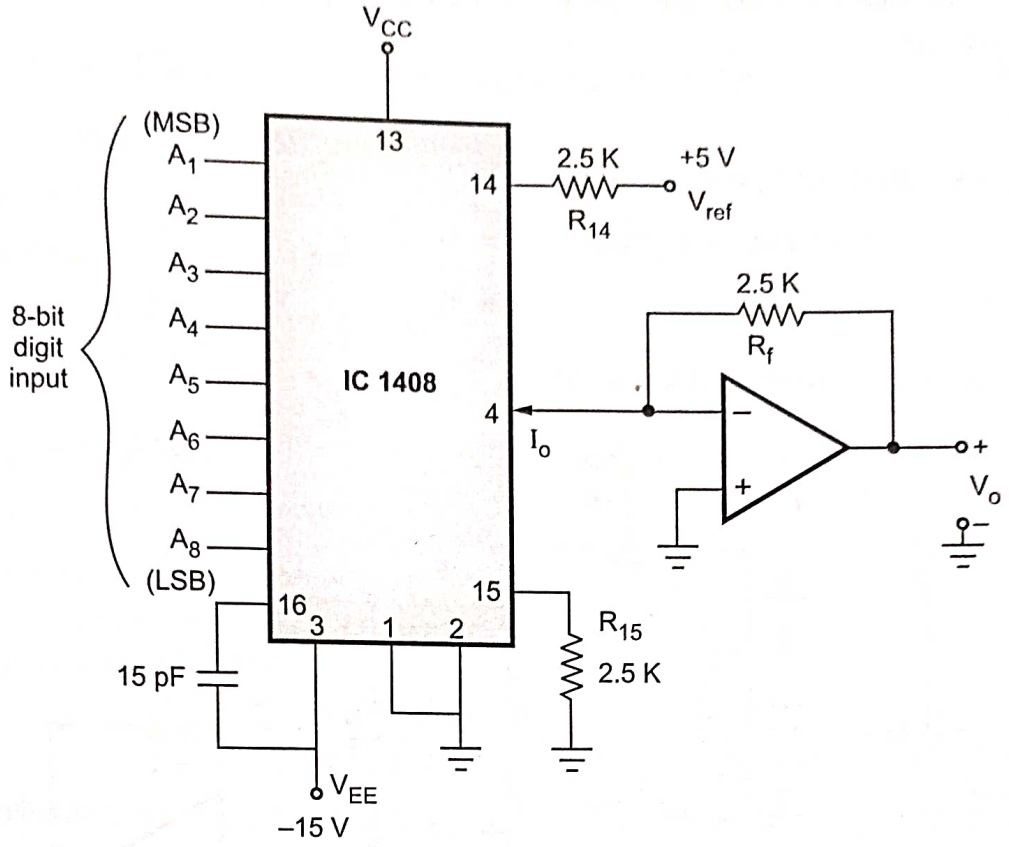

Fig. 8.14 Typical circuit for IC 1408

Note : The arrow on the pin 4 shows the output current direction. It is inward. This means that IC 1408 sinks current. At $(0000\ 0000)_2$ binary input it sinks zero current and at $(1111\ 1111)_2$ binary input it sinks 1.992 mA.

The circuit shown in the Fig. 8.14 gives output in the unipolar range. When digital input is 00H, the output voltage is 0 V and when digital input is FFH $(1111\ 1111)_2$, the output voltage is + 5 V. This circuit can be modified to give bipolar output.

Fig. 8.15 shows the circuit for giving output in the bipolar range. Here, resistor R_B (5 K) is connected between V_{ref} and the output terminal of IC 1408. This gives a constant current source of 1 mA.

The circuit operation can be observed for three conditions :

Condition 1 : For binary input (00H)

When binary input is 00H, the output current I_o at pin 4 is zero. Due to this current flowing through R_B (1 mA) flows through R_f giving $V_o = -5$ V.

Condition 2 : For binary input

When binary input is 80H, the output current I_o at pin 4 is 1 mA. By applying KCL at node A we get,

$$-I_B + I_o + I_f = 0$$

Substituting values of I_B and I_o we get,

$$-(1\text{ mA}) + (1\text{ mA}) + I_f = 0$$

$$\therefore \quad I_f = 0$$

and therefore the output voltage is zero.

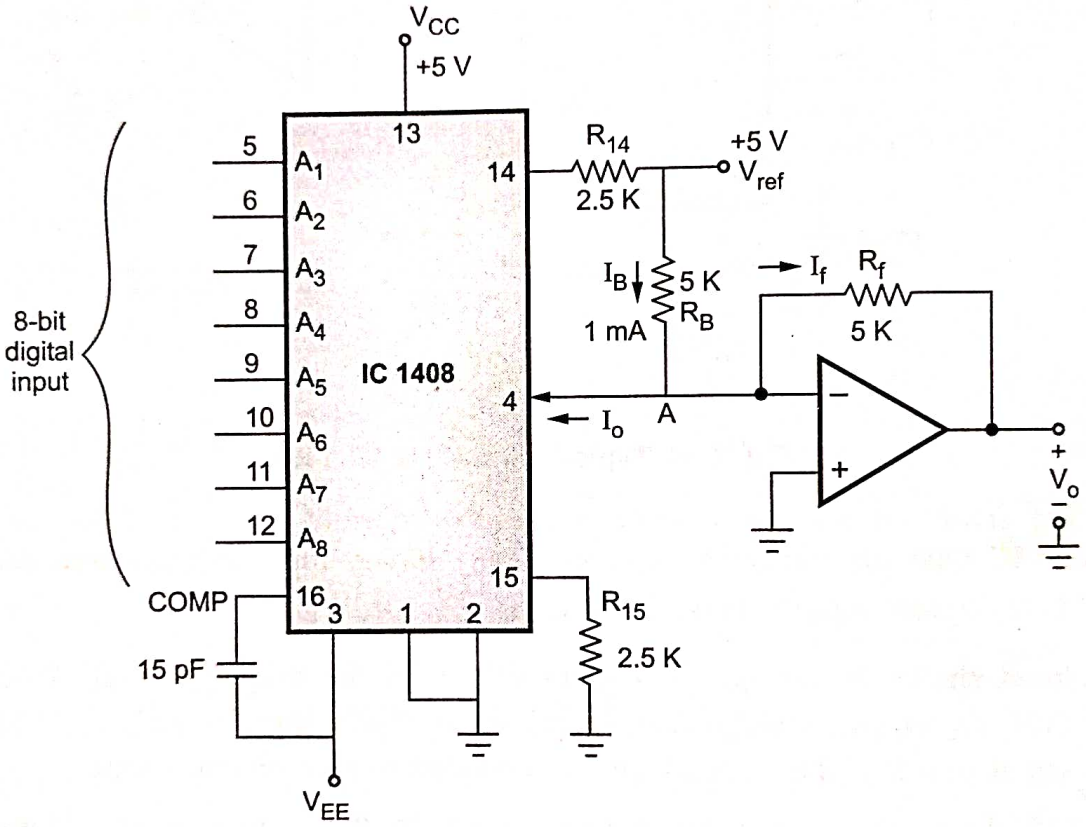

Fig. 8.15 Interfacing DAC in the bipolar range

Condition 3 : For binary input FFH

When binary input is FFH, the output current I_o at pin 4 is 2 mA. By applying KCL at node A we get,

$$-I_B + I_o + I_f = 0$$

Substituting values of I_B and I_o we get,

$$-(1\text{ mA}) + (2\text{ mA}) + I_f = 0$$

$$\therefore \quad I_f = -1\text{ mA}$$

Therefore, the output voltage is + 5 V. In this way, circuit shown in the Fig. 8.15 gives output in the bipolar range.

8.3.1 Important Electrical Characteristics for IC 1408

- Reference current : 2 mA
- Supply voltage : + 5 V_{CC} and – 15 V V_{EE}
- Settling time : 300 ns
- Full scale output current : 1.992 mA
- Accuracy : 0.19 %

8.4 A/D Converters

The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word. Thus the A/D converter is exactly opposite function to that of the D/A converter.

Fig. 8.16 shows symbol for A/D converter.

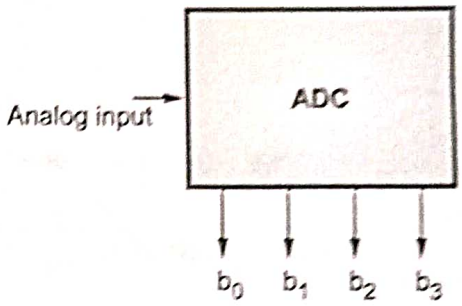

Fig. 8.16 Symbol for 4-bit ADC

8.4.1 Performance Parameters (Specifications) of ADC

The Fig. 8.17 shows the digital output of an ideal 3 bit ADC plotted against the analog input voltage. (See Fig. 8.17 on next page.)

Let us define the performance parameters of ADC, referring to the Fig. 8.17, which shows the output-input characteristics of ADC.

8.4.1.1 Resolution

Fig. 8.17 shows eight (2^3) discrete output states from 000_2 to 111_2, each step being $\frac{1}{8}$ V apart. Therefore, we can say that expression of ADC resolution is the same as for the DAC and is repeated here :

$$\text{resolution} = 2^n \quad \ldots (1)$$

Resolution is also defined as the ratio of a change in value of input voltage, V_i, needed to change the digital output by 1 LSB. If the full scale input voltage required to cause a digital output of all 1's is V_{iFS}, then resolution can be given as

$$\text{resolution} = \frac{V_{iFS}}{2^n - 1} \quad \ldots (2)$$

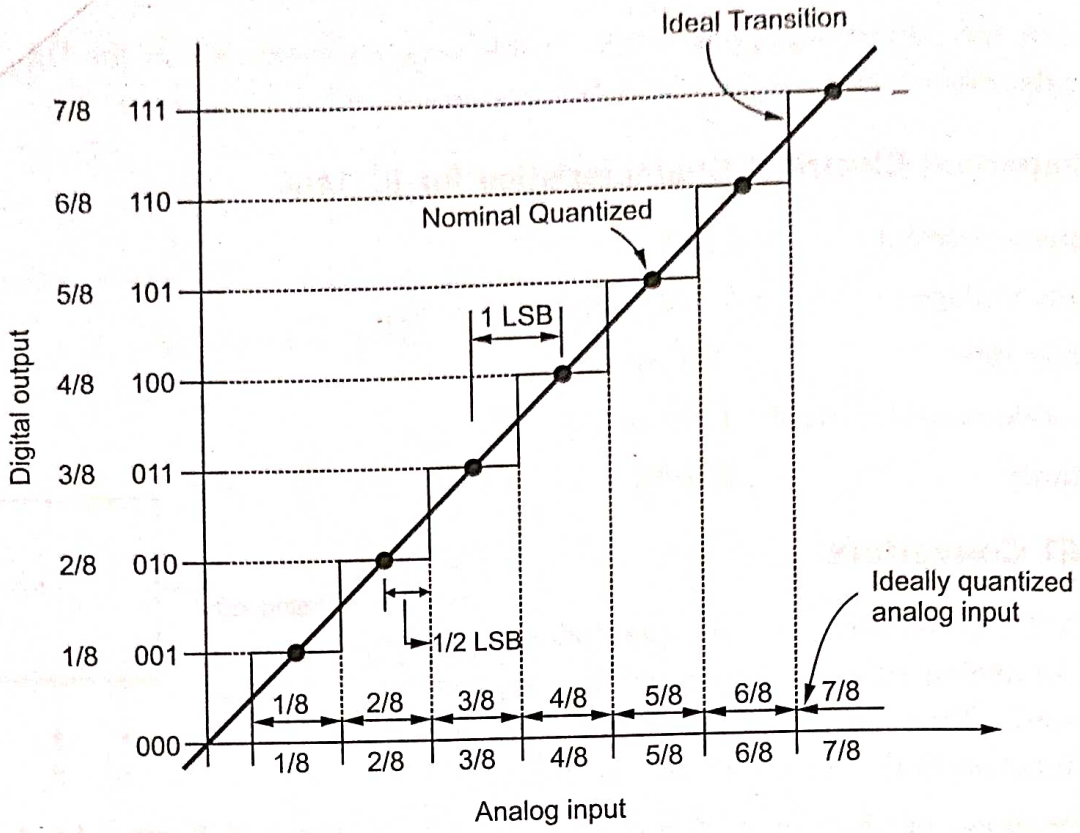

Fig. 8.17 Analog input Vs Digital output

8.4.1.2 Quantization Error

Fig. 8.17 shows that the binary output is 011 for all values of V_i between $\frac{1}{4}$ and $\frac{1}{2}$ V. There is an unavoidable uncertainty about the exact value of V_i when the output is 011. This uncertainty is specified as **quantization error**. Its value is $\pm \frac{1}{2}$ LS B.

It is given as,

$$Q_E = \frac{V_{iFS}}{(2^n - 1)\,2} \quad \ldots (3)$$

Increasing the number of bits results in a finer resolution and a smaller quantization error. The quantization error can be observed by continuously sampling a time-varying analog signal with an ADC, converting it back to analog with a DAC, and taking the difference between the two. The resulting sawtooth-like signal, called **quantization noise**.

The root mean square value of such signal, E_n can be given as

$$E_n = \frac{V_{FS}}{2^n \sqrt{12}}$$

This is related to the resolution of the system. For each additional bit of resolution E_n is cut in half, that is reduced by 6 dB.

8.4.1.3 Gain and Offset Error

The offset error is the difference between the actual and ideal first transition voltages. The term offset; however, implies that all conversions are off by an equal amount. On the other hand, the gain error is the difference between the actual full scale transition voltage and the ideal full-scale transition voltage. This is illustrated in Fig. 8.18.

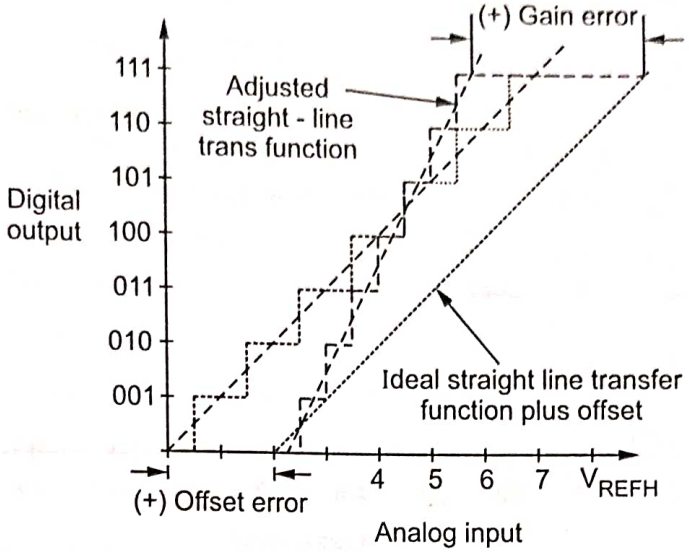

Fig. 8.18 Offset and gain error

8.4.1.4 Gain and Offset Drifts

The gain drift is defined as a change in the full-scale transition voltage measured over the entire operating temperature range. It is usually expressed in parts per million per degree Celsius (ppm/°C).

The offset drift is defined as a change due to temperature in the analog zero for an A/D converter operating in bipolar mode. It is also expressed in parts per million per degree Celsius (ppm/°C).

8.4.1.5 Sampling Frequency and Aliasing Phenomenon

According to sampling theorem, the minimum rate at which the analog signal should be sampled twice the highest frequency in the analog signal. Thus

$$f_s \geq 2f_{max}$$

With this frequency, it is possible to reproduce analog signal faithfully by using a suitable interpolation algorithm.

If the sampling frequency is less than the Nyquist rate ($2\,f_{max}$), then the faithful reproduction of original signal is not possible. However, in such cases, spurious signals called **aliases** are produced. The frequency of aliased signal is the difference between the signal frequency and the sampling frequency. This problem is called **aliasing** and it is removed in all practical A/D converters by using anti-aliasing filters.

8.4.1.6 Non Linearity or Integral Non-Linearity (INL)

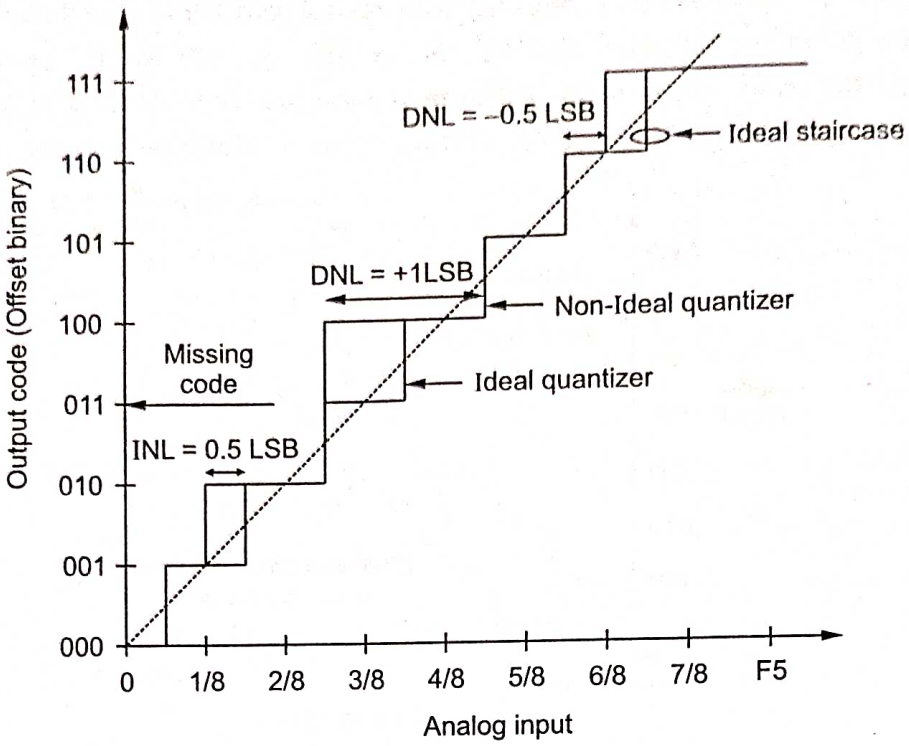

Fig. 8.19 INL and DNL analog input

It is a measure of the maximum deviation of the actual ADC transfer function from a straight line drawn through the first and last code transition after correction for offset and gain errors. It gives a more pessimistic but useful estimation of the non-linearity than referring the linearity of the ADC characteristics to an arbitrary best fit curve drawn through the output codes.

8.4.1.7 Differential Non-Linearity (DNL)

Differential Non-Linearity (DNL) is the maximum of the difference in the each conversion's Current Code Width (CCW) and the Ideal Code Width (ICW).

DNL is the most critical of the measures of an ADC's performance for many control applications since it represents the ADC's ability to relate a small change in input voltage to the correct change in code conversion.

DNL is defined as :

$$\text{Code DNL} = \text{CCW} - \text{ICW}$$

$$\text{DNL} = \text{Max (Code DNL)}$$

8.4.1.8 Conversion Time (Settling Time)

It is an important parameter for ADC. It is defined as the total time required to convert an analog signal into its digital output. It depends on the conversion technique used and the propagation delay of circuit components.

8.4.2 Different Types of ADCs

Analog to digital converter are classified into two general groups based on the conversion techniques. One technique involves comparing a given analog signal with the internally generated reference voltages. This group includes successive approximation, flash, delta modulated (DM), adaptive delta modulated and flash type converters. The another technique involves changing an analog signal into time or frequency and comparing these new parameters against known values. This group includes integrator converters and voltage-to-frequency converters.

In this chapter we are going to discuss following types of ADCs using various conversion techniques :

1. Single ramp or single slope
2. Dual slope
3. Successive approximation
4. Flash
5. Counter type
6. Tracking converter

8.4.2.1 Single Slope ADC

It consists of a ramp generator and BCD or binary counters. The Fig. 8.20 shows the single slope ADC.

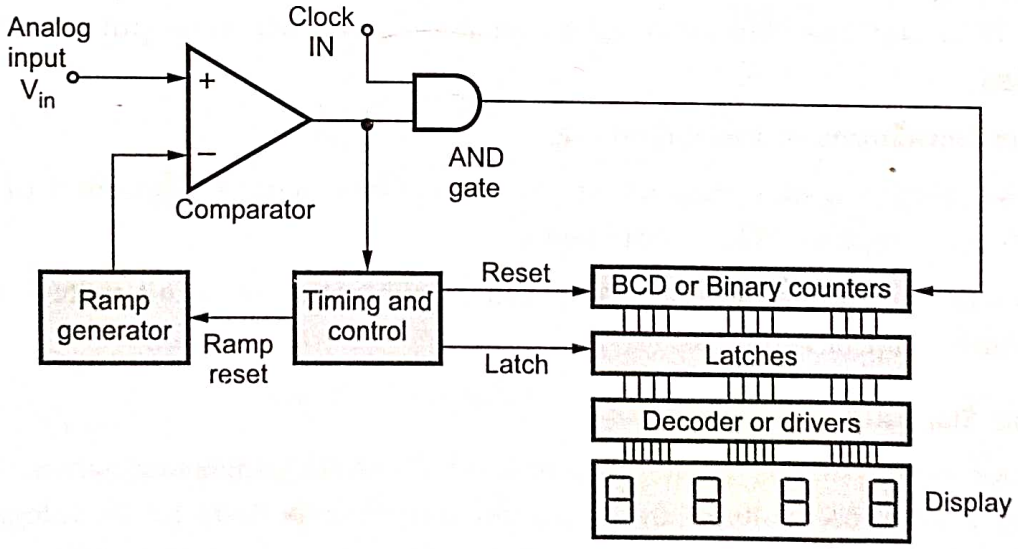

Fig. 8.20 Single slope ADC

At the start, the reset signal is provided to the ramp generator and the counters. Thus counters are reset to 0's. The analog input voltage V_{in} is applied to the positive terminal

of the comparator. As this is more positive than the negative input, the comparator output goes high. The output of ramp generator is applied to the negative terminal of the comparator. The high output of the comparator enables the AND gate which allows clock to reach to the counters and also this high output starts the ramp.

The ramp voltage goes positive until it exceeds the input voltage. When it exceeds V_{in}, comparator output goes low. This disables AND gate which in turn stops the clock to the counters. The control circuitry provides the latch signal which is used to latch the counter data. The reset signal resets the counters to 0's and also resets the ramp generator. The latched data is then displayed using decoder and a display device.

Let us consider the practical example to understand the working. Assume that the clock frequency is 1 MHz. There are four BCD counters and the input V_{in} is 2.000 V.

Now let ramp has a slope of 1 V/ms as shown in the Fig. 8.21. As the input is 2.000 V, the ramp will take 2 ms to reach to 2 V and to stop the clock to the counters.

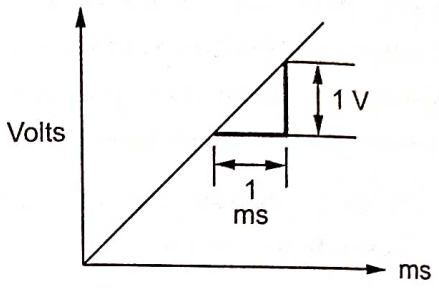

Fig. 8.21

Now how many pulses will reach to the counters during 2 ms ? It can be calculated from the frequency of the clock. The number of pulses reaching to the counter in 2 ms is $\frac{2\text{ ms}}{(1/1\text{ MHz})} = 2000$. The comparator output going high will strobe. The latches and send the count to the displays. Inserting a decimal point at the proper point in the seven segment display gives a reading of 2.000. But we want binary output. In such case instead of BCD counters, binary counters must be used, where output will be straight binary coded.

The main **limitations** of this circuit are,

i) Its resolution is less. Hence for applications which require resolution of 9 part in 20,000 or more, this ADC is not stable.

ii) Variations in ramp generator due to time, temperature or input voltage sensitivity also cause a lot of problems.

8.4.2.2 Dual Slope ADC

Dual slope conversion is an indirect method for A/D conversion where an analog voltage and a reference voltage are converted into time periods by an integrator, and then measured by a counter. The speed of this conversion is slow but the accuracy is high.

Fig. 8.22 shows a typical dual slope converter circuit. It consists of integrator (ramp generator), comparator, binary counter, output latch and reference voltage. The ramp generator input is switched between the analog input voltage V_i and a negative reference voltage, $-V_{REF}$. The analog switch is controlled by the MSB of the counter. When the MSB is a logic 0, the voltage being measured is connected to the ramp generator input. When MSB is logic 1, the negative reference voltage is connected to the ramp generator.

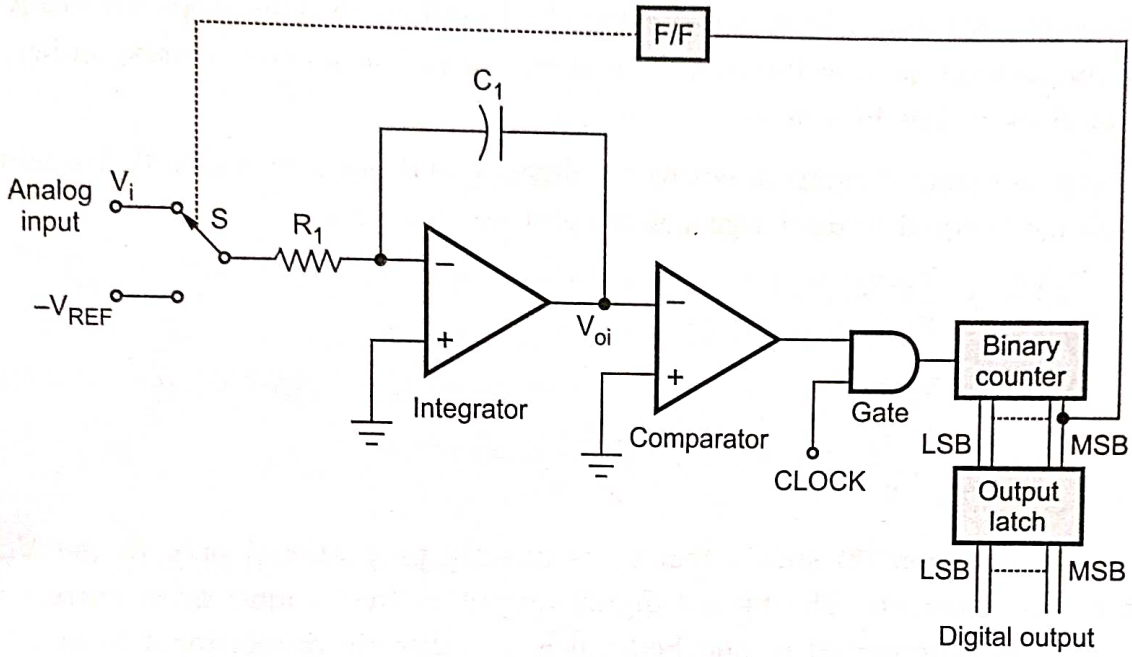

Fig. 8.22 Dual slope A/D converter

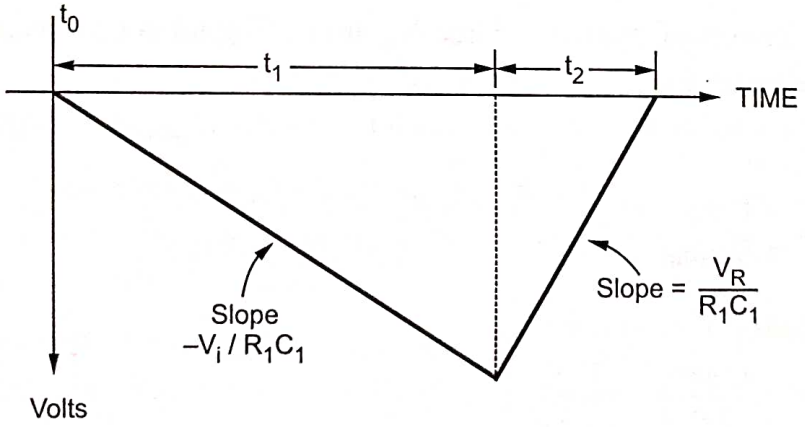

Fig. 8.23 Integrator output voltage

At time t = 0, analog switch S is connected to the analog input voltage V_i, so that the analog input voltage integration begins. The output voltage of the integrator can be given as,

$$V_{oi} = \frac{-1}{R_1 C_1} \int_0^t V_i \, dt = \frac{-V_i \, t}{R_1 C_1} \quad \ldots (4)$$

where $R_1 C_1$ is the integrator time constant and V_i is assumed constant over the integration time period. At the end of 2^N clock periods MSB of the counter goes high. At a result the output of the flip-flop goes high, which causes analog switch S to be switched from V_i to $-V_R$. At this very same time the binary counter which has gone through its entire count sequence is reset.

The negative input voltage ($-V_R$) connected to the input of integrator causes the integrator output to ramp positive. When integrator output reaches zero, the comparator output voltage goes low, which disables the clock AND gate. This stops the clock pulses reaching the counter, so that the counter will be stopped at a count corresponding to the number of clock pulses in time t_2.

The integrator output ramp down to a voltage V and get back up to 0. Therefore, the charge voltage is equal to discharge voltage and we can write,

$$\frac{V_i\, t_1}{R_1\, C_1} = \frac{V_R\, t_2}{R_1\, C_1}$$

$$\therefore \quad V_i\, t_1 = V_R\, t_2$$

$$\therefore \quad t_2 = \frac{V_i\, t_1}{V_R} \qquad \ldots (5)$$

The above equation (5) shows that t_2 is directly proportional only to the V_i, since V_R and t_1 are constants. The binary digital output of the counter gives corresponding digital value for time period t_2 and hence it is also directly proportional to input signal V_i.

The actual conversion of analog voltage V_{in} into a digital count occurs during t_2. The control circuit connects the clock to the counter at the beginning of t_2. The clock is disconnected at the end of t_2. Thus the counter contents is digital output. Hence we can write,

$$\text{Digital output} = \left(\frac{\text{Counts}}{\text{Second}}\right) t_2 \qquad \ldots (6)$$

But from equation (5) we can write,

$$\text{Digital output} = \left(\frac{\text{Counts}}{\text{Second}}\right) t_1 \left(\frac{V_i}{V_R}\right) \qquad \ldots (7)$$

The counter output can then be connected to an appropriate digital display.

The advantages of dual slope ADC are

1. It is highly accurate.
2. Its cost is low.
3. It is immune to temperature caused variations in R_1 and C_1.

The only disadvantage of this ADC is its speed which is low.

Example 8.8 *For a particular dual slope ADC, t_1 is 83.33 ms and the reference voltage is 100 mV. Calculate t_2 if i) V_i is 100 mV and ii) 200 mV.*

Solution : We know that,

$$t_2 = \left(\frac{V_i}{V_R}\right) t_1$$

i) $$t_2 = \left(\frac{100}{100}\right)(83.33) = \mathbf{83.33\ ms}$$

ii) $$V_i = 200\ \text{mV}$$

$$\therefore \quad t_2 = \left(\frac{200}{100}\right)(83.33) = \mathbf{166.6\ ms}$$

Example 8.9 *Find the digital output of an ADC having t_1 as 83.33 ms and V_R as 100 mV for an input voltage of + 100 mV. The clock frequency is 12 kHz.*

Solution : The digital output is given as,

$$\text{Digital output} = \left(\frac{\text{Counts}}{\text{Second}}\right) t_1 \left(\frac{V_i}{V_R}\right)$$

Now Clock frequency = 12 kHz

$$\text{i.e.} = 12000\ \frac{\text{Counts}}{\text{Second}}$$

$$\therefore \quad \text{Digital output} = 12000 \times 83.33 \times \left(\frac{100}{100}\right) \times 10^{-3} = 1000 \text{ counts.}$$

8.4.2.3 Successive Approximation ADC

In this technique, the basic idea is to adjust the DAC's input code such that its output is within ± ½ LSB of the analog input V_i to be A/D converted. The code that achieves this represents the desired ADC output.

The successive approximation method uses very efficient code searching strategy called binary search. It completes searching process for n-bit conversion in just n clock periods.

Fig. 8.24 shows the block diagram of successive approximation A/D converter. It consists of a DAC, a comparator, and a Successive Approximation Register (SAR).

The external clock input sets the internal timing parameters. The control signal start of conversion (SOC) initiates an A/D conversion process and end of conversion signal is activated when the conversion is completed.

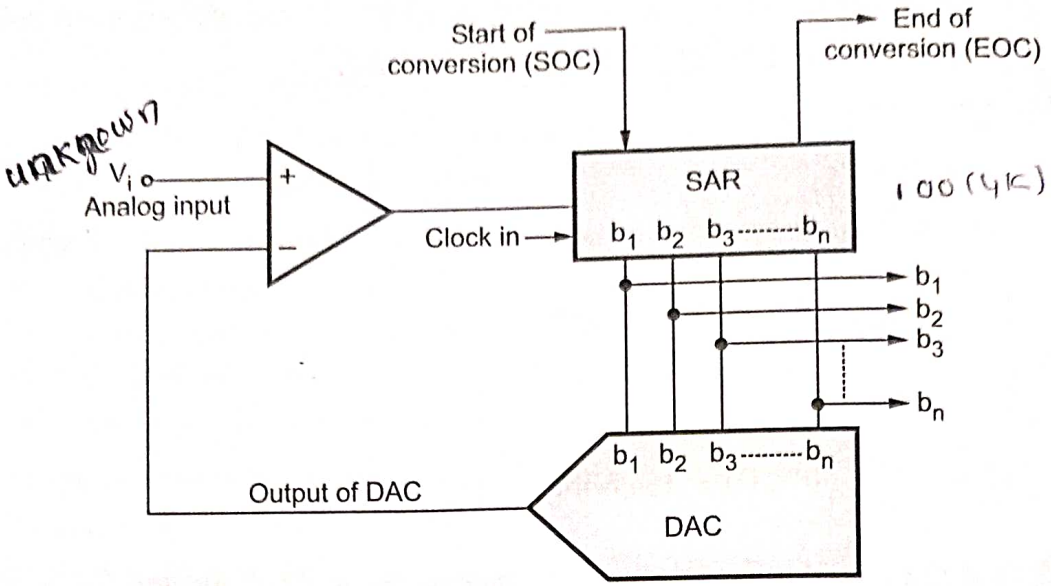

Fig. 8.24 Block diagram of successive approximation A/D converter

Operation :

The searching code process in successive approximation method is similar to weighing an unknown material with a balance scale and a set of standard weights. Let us assume that we have 1 kg, 2 kg and 4 kg weights (SAR) plus a balance scale (comparator and DAC). Now we will see the successive approximation analogy for 3-bit ADC.

Refer Fig. 8.24 and 8.25. The analog voltage V_{in} is applied at one input of comparator. On receiving start of conversion signal (SOC) successive approximation register sets 3-bit binary code 100_2 ($b_2 = 1$) as an input of DAC. This is similar process of placing the unknown weight on one platform of the balance and 4 kg weight on the other. The DAC converts the digital word 100 and applies it equivalent analog output at the second input of the comparator. The comparator then compares two voltages just like comparing unknown weight with 4 kg weight with the help of balance scale. If the input voltage is greater than the analog output of DAC, successive approximation register keeps $b_2 = 1$ and makes $b_1 = 1$ (addition of 2 kg weight to have total 6 kg weight) otherwise it resets $b_2 = 0$ and makes $b_1 = 1$ (replacing 2 kg weight). The same process is repeated for b_1 and b_0. The status of b_0, b_1 and b_2 bits gives the digital equivalent of the analog input. Fig. 8.25 illustrates the process we have just discussed.

The dark lines in the Fig. 8.25 shows setting and resetting actions of bits for input voltage 5.2 V, on the basis of comparison. It can be seen from the Fig. 8.25 that one clock pulse is required for the successive approximation register to compare each bit. However an additional clock pulse is usually required to reset the register prior to performing a conversion.

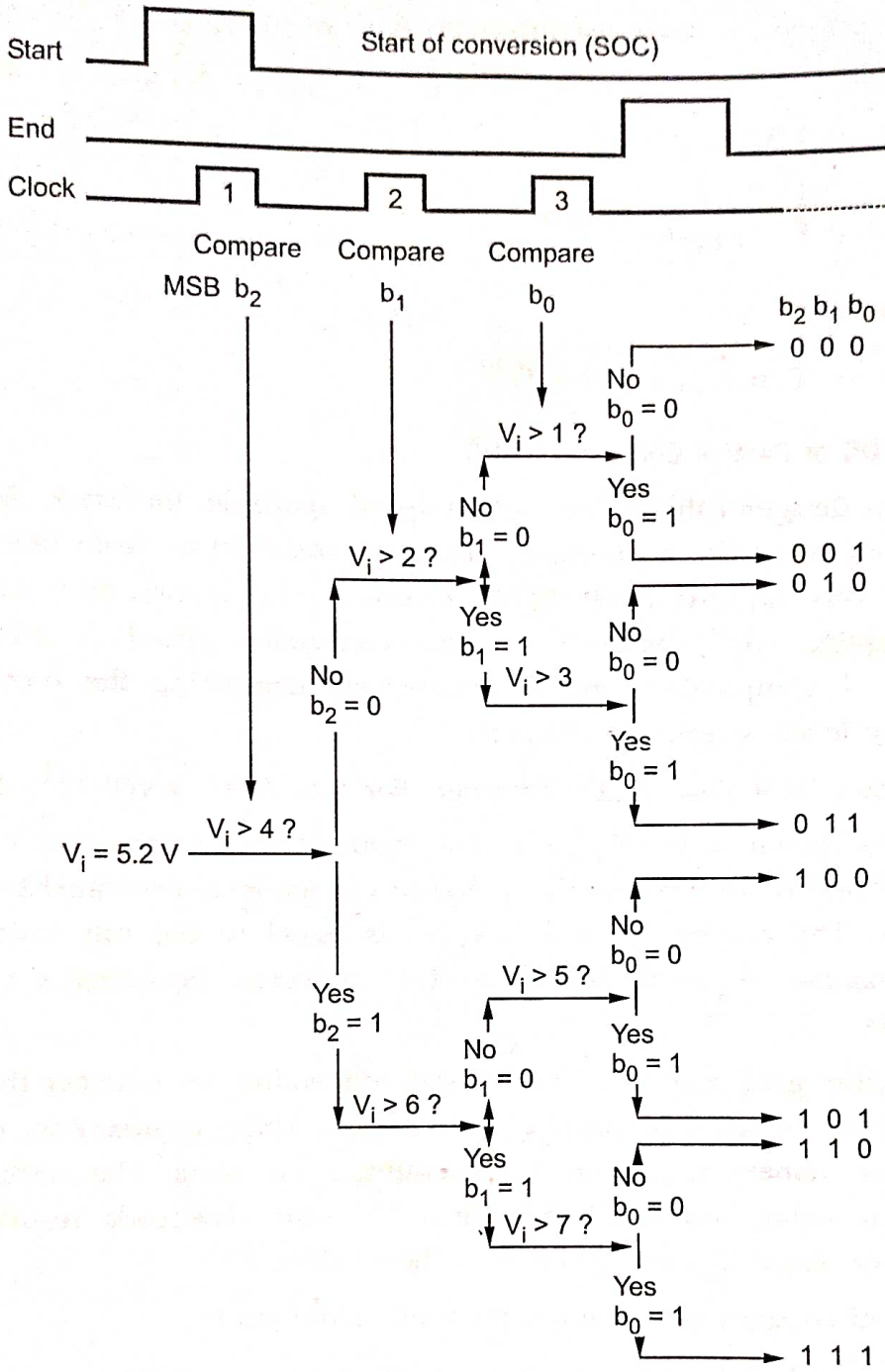

Fig. 8.25 Illustration of conversion process

The time for one analog to digital conversion must depend on both the clock's period T and number of bits n. It is given as,

$$T_C = T (n + 1) \quad \ldots(8)$$

where T_C = Conversion time

T = Clock period

n = Number of bits

Example 8.10 *An 8 bit successive approximation ADC is driven by a 1 MHz clock. Find its conversion time.*

Solution : $f = 1$ MHz

$$\therefore \quad T = \frac{1}{f} = \frac{1}{1\times10^6} = 1\ \mu\text{sec}$$

$$n = 8$$

$$\therefore \quad T_C = T\,(n + 1) = 1\,(8 + 1) = 9\ \mu\text{sec.}$$

8.4.2.4 Flash ADC or Parallel Comparator ADC

When system designs call for the highest speed available, flash-type A/D converters (ADCs) are likely to be the right choice. They get their names from their ability to do the conversion very rapidly. Flash A/D converters, also known as a simultaneous or parallel comparator ADC, because the fast conversion speed is accomplished by providing $2^n - 1$ comparators and simultaneously comparing the input signal with unique reference levels spaced 1 LSB apart.

Fig. 8.26 shows 3-bit flash A/D converter. For this ADC, seven $(2^3 - 1)$ comparators are required. As shown in the Fig. 8.26, one input of each comparator is connected to the input signal and other input to the reference voltage level generated by the reference voltage divider. The reference voltage (V_{REF}) is equal to the full scale input signal voltage. The manner in which the flash A/D converter performs a quantization is relatively simple.

The comparators give output "1" or "0" state depending on whether the input signal is above or below the reference level at that instant. Those comparators referred above the input signal, remain turned-off, representing a "0" state. The comparators at or below the input signal conversely become a "1" state. The code resulting from this comparator is converted to a binary code by the encoder.

The number of comparators required for n bit resolution is,

$$\text{Number of comparators} = 2^n - 1 \qquad \ldots (9)$$

As seen earlier the quantization error is $\pm \frac{1}{2}$ LSB. Thus for an ADC, the maximum frequency for a sine wave V_{in} to be digitized within an accuracy of $\pm \frac{1}{2}$ LSB is,

$$f_{max} \cong \frac{1}{2\pi(T_C)2^n} \qquad \ldots (10)$$

where f_{max} = Maximum input frequency

T_C = Conversion time

n = Number of bits

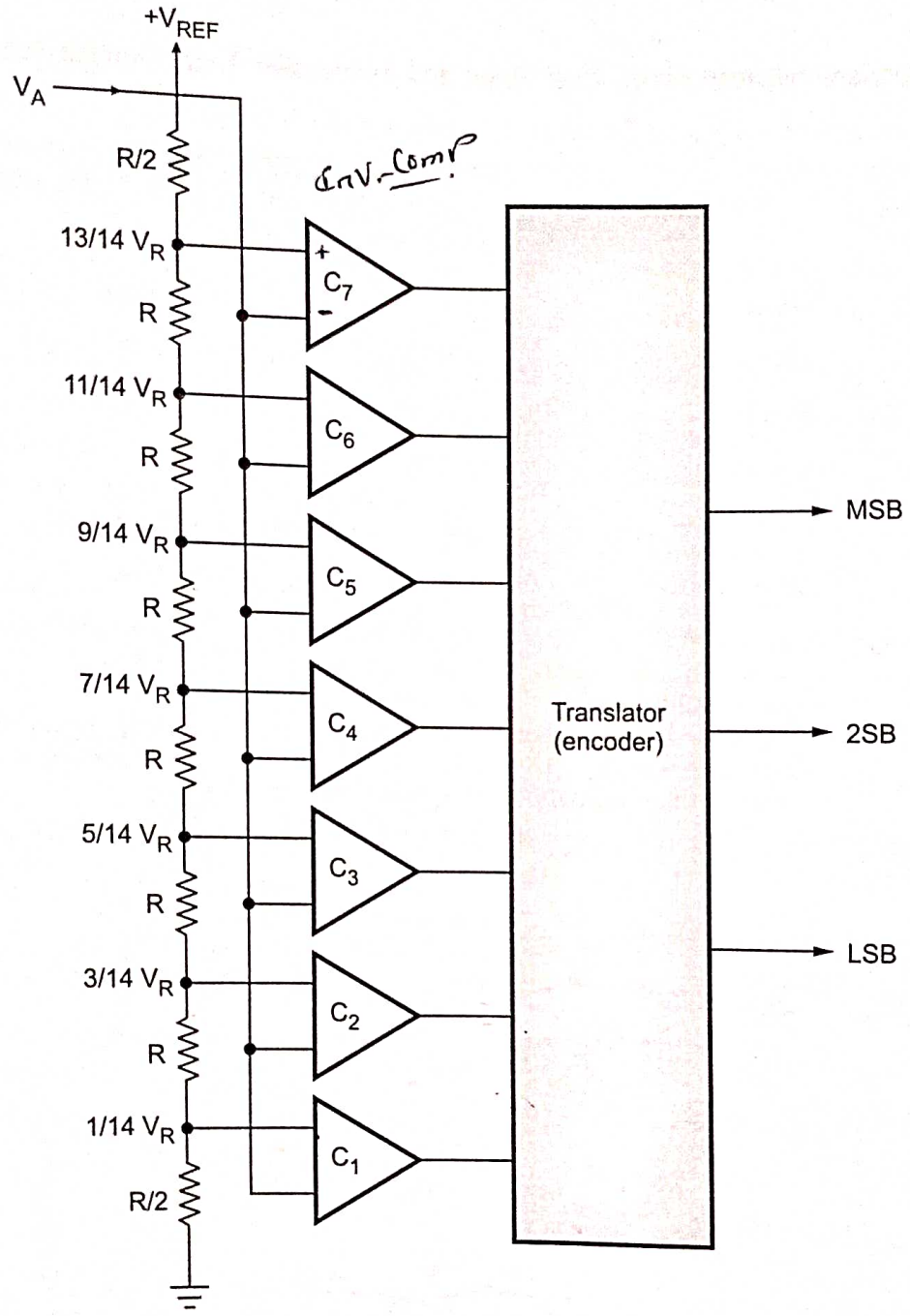

Fig. 8.26 3-bit flash converter

Example 8.11 *For a particular 8-bit ADC, the conversion time is 9 μs. Find the maximum frequency of an input sine wave that can be digitized.*

Solution : The maximum frequency is given by,

$$f_{max} \approx \frac{1}{2\pi(T_C)2^n} \approx \frac{1}{2\pi \times 9 \times 10^{-6} \times 2^8} \approx 69.07 \text{ Hz}$$

8.4.2.5 Comparison between Flash, Dual Slope and Successive Approximation Techniques

The comparison of ADCs is given in the tabular form as below :

Parameter	Flash	Successive approximation	Dual slope
Speed	Fastest	Fast	Slow
Accuracy	Less	Medium	More
Resolution	Upto 2^8	Upto 2^{16}	2^{16} or even more
Input hold time	Very less	Depend on number of bits. It is more than flash A/D converter.	It is maximum, hence sample and hold circuit is required.
Cost	Very costly	Medium	Less
Applications	High speed fiber optic communication, Digital storage oscilloscope, Imaging and many more where high speed A/D conversion is required.	The successive approximation A/D converter has the disadvantage of requiring D/A converter, but it has the advantage of high speed with excellent resolution. Hence these are most popular and used in data acquisition systems.	These are used when high accuracy and resolution is required and speed is not the important criteria.

	IC	Resolution	Conversion rate	IC	Resolution	Conversion rate	IC	Resolution	Conversion rate
ICs	AD6020KD	6	50 MHz	ADC1103	8	1 MHz	ADC141	14	25 Hz
	AD9000SD	6	75 MHz	ADC60	10	670 kHz	7109	12	30 Hz
	TM1070	7	15 MHz	ADC1103	12	300 kHz	ADB1200	12	28 Hz
	TDC10193	9	25 MHz	ADC72	16	20 kHz	LF13300	12	28 Hz

8.4.2.6 Counter Type ADC

Principle of operation

This ADC uses DAC for A to D conversion. The output of the DAC is continuously compared with the analog input to the ADC which is to be converted into digital output. When the output of the DAC becomes greater than this analog input, the corresponding digital input to the DAC is noted which represents the analog input to the ADC.

Fig. 8.27 shows the circuit diagram of counter type ADC. As shown in the Fig. 8.27, the counter type ADC consists of a binary counter, DAC, comparator and AND gate. The operation of the circuit is explained below.

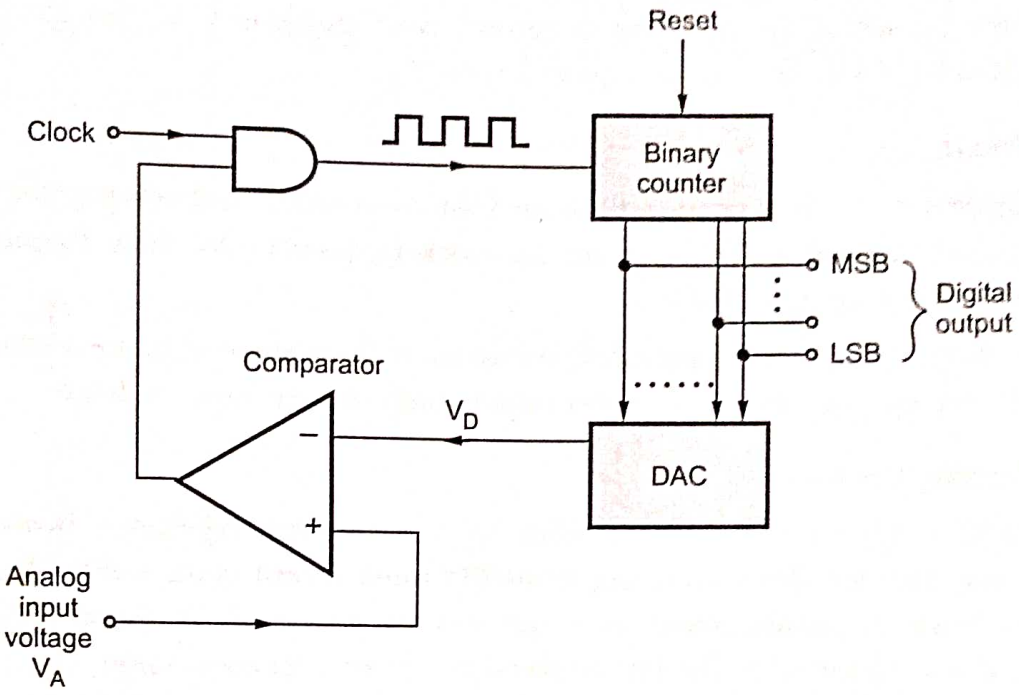

Fig. 8.27

i. Initially, the counter is reset, i.e. its output is set to zero by applying a reset pulse. The output of the counter is given as digital input to DAC. Since input to DAC is zero, its output V_D is zero.

ii. When the analog input voltage V_A is applied to ADC, it becomes greater than V_D. V_A acts as input voltage for non inverting terminal and V_D acts as input voltage for inverting terminal of the comparator. Since V_A is greater than V_D, the comparator output goes high.

iii. For an AND gate, one input is clock pulses and another input is the output of the comparator. Because of the high output of the comparator, the clock pulses are allowed to pass through the AND gate.

iv. The counter starts counting these close pulses. According to the number of clock pulses, the output of the counter goes on increasing. This increases the output of the DAC.

v. The above steps are continued till V_D is less than V_A.

vi. As soon as DAC output V_D becomes greater than V_A, the comparator output goes low. This disables AND gate. So the clock pulses are not allowed to pass through the AND gate. The counting process of the binary counter is stopped.

vii. The output of the binary counter which is in digital form is noted which represents the digital equivalent of the analog input voltage V_A.

viii. For the next A to D conversion, the input voltage to ADC, V_A changes. The binary counter is cleared by applying a second reset pulse and all the above steps are repeated to obtain the digital equivalent of V_A.

Disadvantages

- It is necessary to give enough time for DAC conversion and comparator to respond. Therefore, there is a limitation on the clock frequency. As clock frequency is low, the speed of conversion is less.
- Conversion time is not constant. It increases with increase in input voltage. In other words, we can say that conversion time is high at high input voltage.

8.4.2.7 Tracking Converter

The tracking type converter is similar to counter type converter; however in this converter the counter starts counting from the **most recent code** rather than restarting from zero. Such an arrangement increases conversion speed, if **signal** changes in the input signal are minor since the last conversion. Increase in conversion speed is achieved because fewer counts are required for the DAC output to catch up with V_i when input changes are minor.

The tracking type converter is also called **servo converter** or **continuous A/D converter.** The Fig. 8.28 shows the tracking type ADC. It consists of up/down counter, a comparator, DAC and the control circuitry. Here, comparator output controls the direction of count. Counting will be up or down depending on whether the DAC output is below or above V_i, i.e. comparator output is logic 0 or logic 1. Whenever, the DAC output crosses V_i, the comparator changes state and generates positive going or negative going edge at the output. This edge can be taken as EOC command, so that counter stops counting when comparator changes its state. The edge detection is achieved by using two D flip-flops. Flip-flop 1 is used to detect positive edge whereas flip-flop 2 is used to detect negative edge. Initially, with the activation of start of conversion (SOC) signal the output of both flip-flops are set to logic 1. Since, the D input of both the flip-flops is connected to logic 0, upon detection of the edge, the flip-flop output goes to logic 0 and disables the clock. As a result, the counter stops counting. When comparator output goes from logic 1 to logic 0, negative edge is generated and it resets flip - flop 2 whereas when comparator output goes from logic 0 to logic 1, positive edge is generated and it resets flip-flop 1. When either of the two flip-flop gets reset, the clock is disabled.

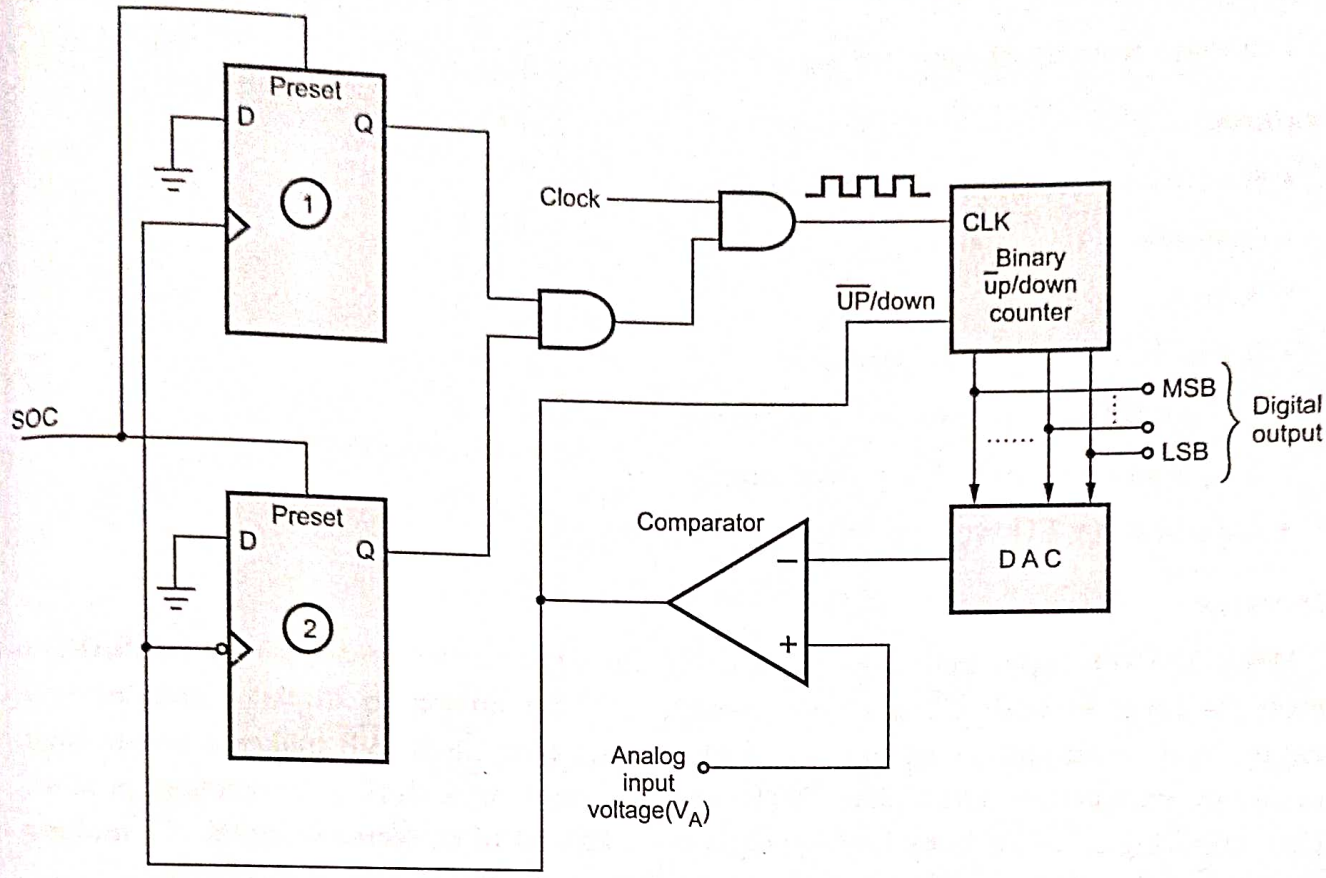

Fig. 8.28 Tracking type ADC

8.5 A/D Converter ICs

ADC 0803 Family

The ADC 0803 and ADC 0805 are CMOS 8-bit successive-approximation analog to digital converters. These devices are design to operate from common microprocessor control buses, with tri-state output latches driving the data bus.

Fig. 8.29 shows the pin diagram of ADC 0803 and ADC 0805.

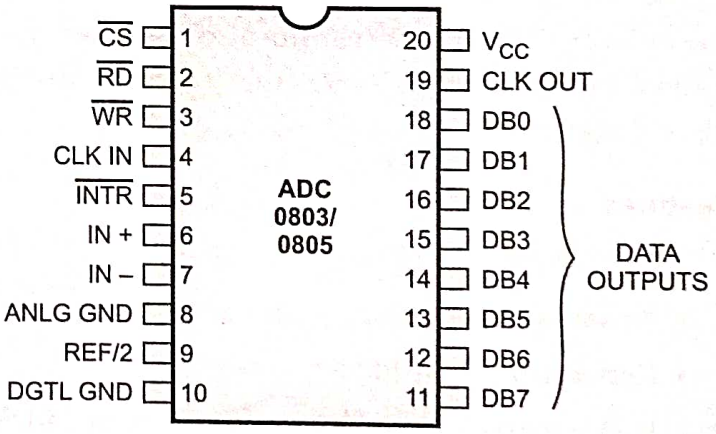

Fig. 8.29 Pin diagram of ADC0803/0805

IN+ and IN– inputs allow application of differential input voltage which has high common mode rejection and eliminates offset due to the zero input analog voltage value. The devices can operate with an external clock signal or, the on chip clock generator can be used independently by adding an external resistor and capacitor to set the time period.

The main features of these family are :

Features

- 8-bit successive approximation ADC
- Conversion time 100 μs
- Access time 135 ns
- It has an on-chip clock generator
- It does not require any zero adjustment.
- It operates on single 5 V power supply
- Output meet TTL voltage level specifications.

Operation

When the $\overline{WR}$ input goes low, the internal successive approximation register (SAR) is reset. As long as both $\overline{CS}$ and $\overline{WR}$ remain low, the analog to digital converter will remain in its reset state. One to eight clock periods after $\overline{CS}$ or $\overline{WR}$ makes a low-to-high transition, conversion starts. The $\overline{INTR}$ signal is held high during conversion process. After conversion, $\overline{INTR}$ goes low which is used as end of conversion signal. By making $\overline{CS}$ and $\overline{RD}$ signals low, an output can be read through DB0 to DB7 data signals.

ADC 0808/0809 Family

The ADC 0808 and ADC 0809 are monolithic CMOS devices with an 8-channel multiplexer. These devices are also designed to operate from common microprocessor control buses, with tri-state output latches driving the data bus. The main features of these devices are :

Features

- 8-bit successive approximation ADC.
- 8-channel multiplexer with address logic.
- Conversion time 100 μs.
- It eliminates the need for external zero and full-scale adjustments.
- Easy to interface to all microprocessors.
- It operates on single 5V power supply.
- Output meet TTL voltage level specifications.

Fig. 8.30 shows pin diagram of 0808/0809 ADC.

ADC 0808/0809 has eight input channels, so to select desired input channel, it is necessary to send 3-bit address on A, B and C inputs. The address of the desired

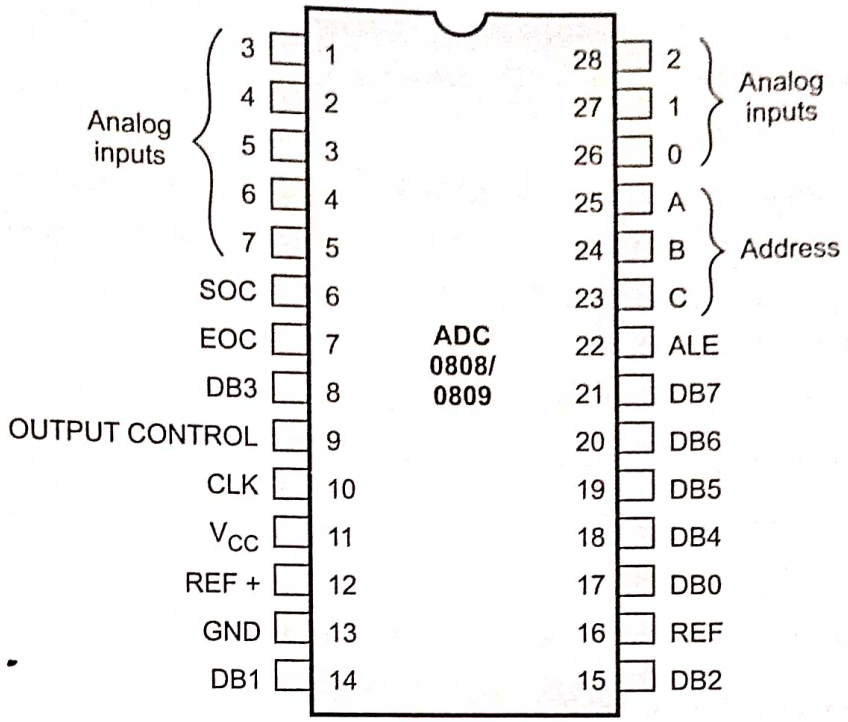

Fig. 8.30 Pin diagram of 0808/0809

channel is sent to the multiplexer address inputs through port pins. After at least 50 ns, this address must be latched. This can be achieved by sending ALE signal. After another 2.5 µs, the start of conversion (SOC) signal must be sent high and then low to start the conversion process. To indicate end of conversion ADC 0808/0809 activates EOC signal. The microprocessor system can read converted digital word through data bus by enabling the output enable signal after EOC is activated. This is illustrated in Fig. 8.31.

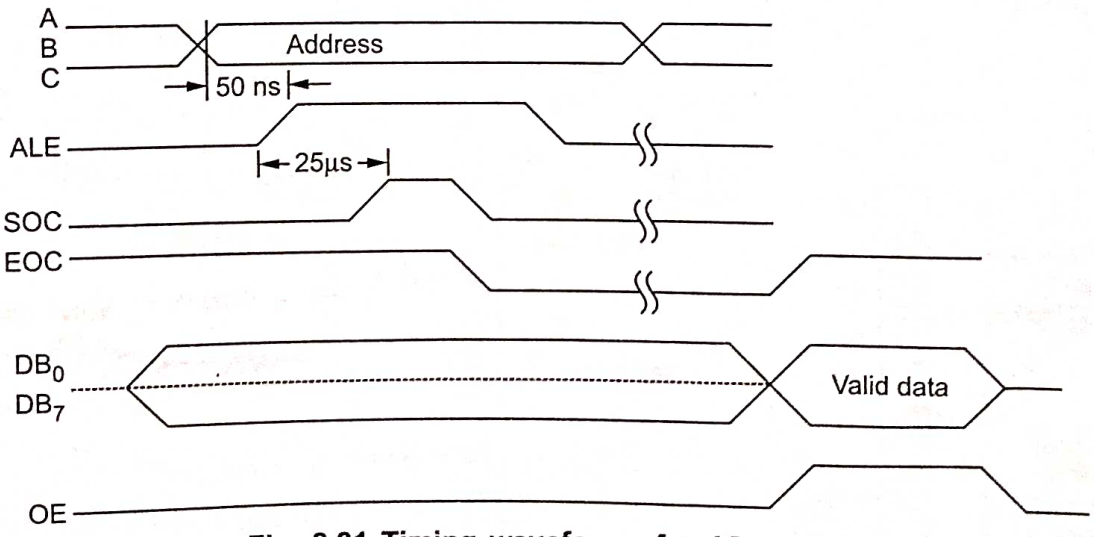

Fig. 8.31 Timing waveforms for ADC 0808

IC 7109

The ICL 7109 is a high performance, low power integrating (Dual slope) A/D converter designed to easily interface with microprocessor.

Features

- IC 7109 is a 12-bit dual slope A/D converter.
- It has polarity and over range bits.
- It has byte organized TTL compatible three-state outputs and UART handshake mode for simple parallel or serial interfacing to microprocessor systems.
- It has $\overline{\text{RUN}}$/HOLD input and STATUS output, which can be used to monitor and control conversion timing.
- It has true differential input and differential reference
- It has low noise-typically 15 μV_{p-p}.
- It has very low input current - 1pA
- It operates at 30 conversions per second.
- All inputs are fully protected against static discharge.

Pin Configuration and Test Circuit

The Fig. 8.32 shows typical circuit and pin configuration for 7109.

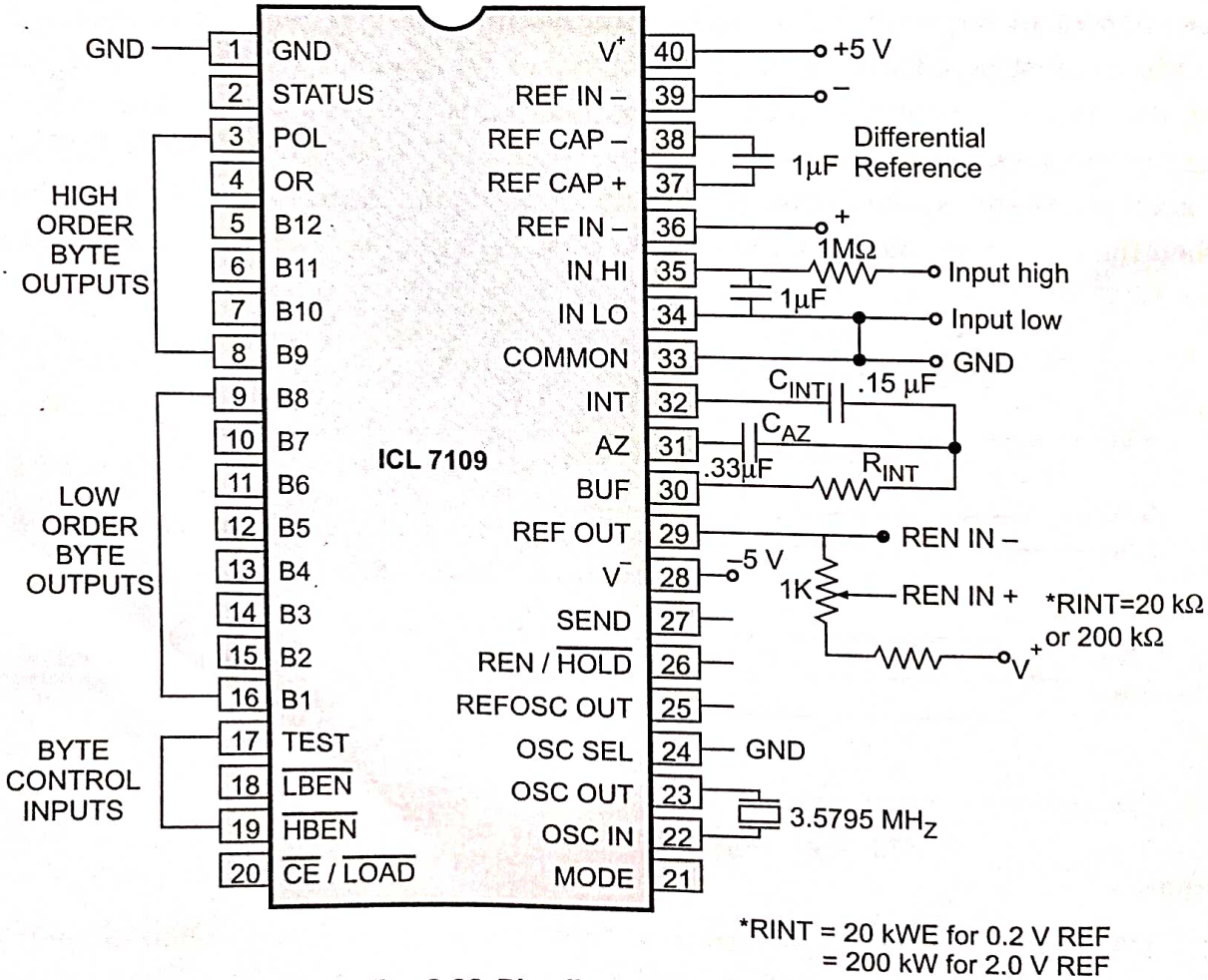

Fig. 8.32 Pin diagram of ICL 7109

8.6 AD574A (12-bit A/D Converter) Specifications

The AD574A is a complete 12-bit A/D converter which requires no external components to provide the complete successive approximation analog-to-digital conversion function. The specifications of AD574AJ are as shown in Table 8.1.

Parameter	Value
Resolution	12-bit
Linearity Error	± 1 LSB
Temperature range	0 – 70 °C
Analog input range	– 5 to 5 V
Power supply :	
V_{Logic}	+4.5 to +5.6
V_{CC}	+11.4 to +16.5
V_{EE}	–11.4 to –16.5
Power Dissipation	390 mW (Typical)
	725 mW (Maximum)
Internal reference voltage	9.98 to 10.02
Maximum conversion time	35 µs
Operating current	
I_{LOGIC}	30 - 40 mA
I_{CC}	2 - 5 mA
I_{EE}	18 - 30 mA

Table 8.1 Specification of AD574AJ

Solved Examples

Example 8.12 *The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0 V, what is the output for an input of 101101111?*

Solution : The output for an input of 101101111_2 (367_{10}) = 10.3 mW × 367 = 3.7801 V

Example 8.13 *A dual slope ADC uses a 16 bit counter and a 4 MHz clock rate. The maximum input voltage is +10 V. The maximum integrator output voltage should be –8 V when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1 μF. Find the value of the resistor R of the integrator. If the analog signal is + 4.129 V, find the corresponding binary number.*

Solution : Given $V_{oi} = -8\ V,\ V_i = 10\ V,\ C_1 = 0.1\ \mu F$ and

$$t = 2^N \times 1/4\ MHz = 2^{16} \times 1/4\ MHz = \mathbf{16.384 \times 10^{-3}}$$

i) We know that, the output voltage of the integrator is given as

$$V_{oi} = \frac{-V_i\ t}{R_1\ C_1}$$

$$\therefore \quad R_1 = \frac{-V_i\ t}{V_{oi}\ C_1} = \frac{-10 \times 16.384 \times 10^{-3}}{-8 \times 0.1 \times 10^{-6}} = 204.8\ k\Omega$$

ii) $$\text{Number} = \frac{2^{16} \times 4.129}{10} = 27059.8 \approx 27060 = \mathbf{(0110\ 1001\ 10110100)_2}$$

Example 8.14 *How many bits are required to design a D/A converter, that can have a resolution of 5 mV? The ladder has +8 V full scale.*

Solution : $$\text{Resolution} = \frac{V_{oFS}}{2^n - 1}$$

$$\therefore \quad 2^n = \frac{V_{oFS}}{\text{Resolution}} + 1 = \frac{8\ V}{5mV} + 1$$

$$\therefore \quad n = 10.644 \approx \mathbf{11}$$

Example 8.15 *If the maximum output voltage of a 7 bit D/A converter is 25.4 V, what is the smallest change in the output as the binary count increases ?*

Solution : The smallest change in the output as the binary count increases (Resolution) is given as

$$= \frac{V_{oFS}}{2^n - 1} = \frac{25.4}{2^7 - 1} = \frac{25.4}{128 - 1} = \frac{25.4}{127} = \mathbf{0.2\ V}$$

Example 8.16 *Determine the output voltage produced by a 4 bit DAC whose output voltage range is 0 to 10 V when the input binary number is 0110.*

Solution : Given : $V_{oFS} = 10\ V$

$$\therefore \quad \text{Resolution} = \frac{10}{2^4 - 1} = 0.6667\ V$$

The output voltage at 0110 = $0.6667 \times 6 = \mathbf{4\ V}$

Example 8.17 *Determine the resolution of an 8 bit A/D converter for a 10 V input range.*

Solution : $V_{iFS} = 10$ V

$$\therefore \quad R = \frac{V_{iFS}}{2^n - 1} = \frac{10}{2^8 - 1} = \frac{10}{255} = \mathbf{39.215\ mV}$$

Example 8.18 *The LSB of a 10-bit DAC is 20 mvolts.*

i) What is its percentage resolution ?
ii) What is its full-scale range ?
iii) What is the output voltage for an input, 10110 01101 ? **May-05, Set-1**

Solution : i) $20 \times 10^{-3} \times 100 = 2\ \%$

$$V_{oFS} = (2^n - 1) \times \text{Resolution} = 20.46\ V$$

ii) $(101100\ 1101)_2 = 717$

$$\therefore \quad V_o = 717 \times 20 \times 10^{-3} = 14.34\ V$$

Example 8.19 *LSB of 9-bit DAC is represented by 19.6 volts. If an input of 9 zero bits is represented by 0 volts.*

i) Find the output of the DAC for an input, 10110 1101 and 01101 1011.

ii) What is the Full Scale Reading (FSR) of this DAC ? **May-05, Set-3**

Solution : i) $(10110\ 1101)_2 = (365)_{10}$

$(01101\ 1011)_2 = (219)_{10}$

$\therefore$ Input 10110 1101 gives output

$$= 365 \times 19.6 \times 10^{-3} = 7.154\ V$$

and input 01101 1011 gives output

$$= 219 \times 19.6 \times 10^{-3} = 4.2924\ V$$

ii) $V_{oFS} = (2^9 - 1) \times \text{Resolution} = (2^9 - 1) \times 19.6 \times 10^{-3} = 10\ V$

Example 8.20 *Calculate the conversion time for a full scale input in case of a 12-bit counter type analog to digital converter driven by 2 MHz clock.* **May-05, Set-3**

Solution : $T = \frac{1}{2 \times 10^6} = 0.5\ \mu s$

The total time for a full scale input in case of a 12-bit counter type $= (2^n - 1) \times T$

$$= (2^{12} - 1) \times 0.5\ \mu s = 2.0475\ ms$$