CMOS Logic

→ The basic building of CMOS logic ckt is MOS transistor. As we know, logic ckts (or) Digital ckts procies the binary digits i.e '1' & '0', However, Real logic ckts process Electrical signals as voltage levels.

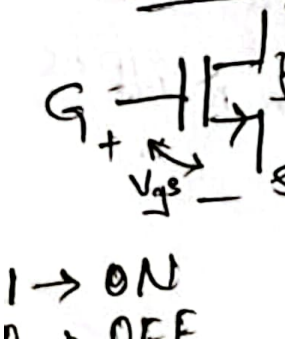
→ In any logic ckt, there is a range of voltages for Logic '0' & Logic '1'. A typical CMOS, operates from 5V power supply. It may have Logic '0' → 0 to 1.5V in b/w these, are the Undefined Logic '1' → 3.5 to 5V. Logic Levels.

MOS Transistor :- which is having three terminals G, D, S. As the name it implies, the Electric field applied at the 'Gate' terminal will Control the flow of current b/w drain & Source (or) it will Controls the resistance b/w → So, it is used as voltage Controlled resistance.

→ In digital applications when MOS transistor is 'OFF', then its resistance is 'very high'; & when it is 'ON', then its resistance "very low"

→ There are two types → PMOS
→ NMOS → is the most widely used

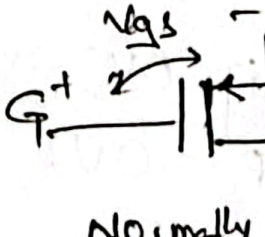
NMOS



As V_{gs} ↑ ⇒ R_{ds} ↓
Normally $V_{gs} \geq 0$.
i.e '0' (or) +ve

1 → ON
0 → OFF

PMOS



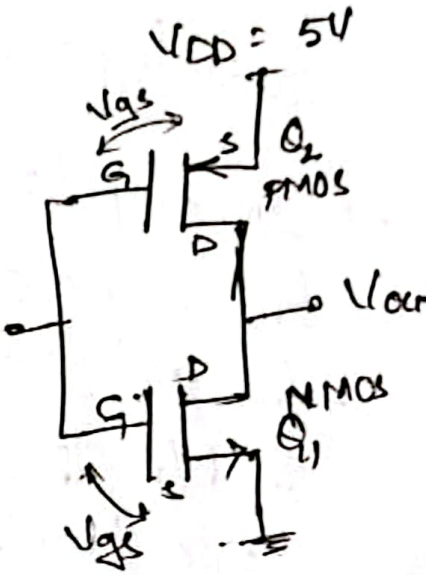
'1' → OFF
'0' → ON.
$V_{gs} = 0 \Rightarrow R_{ds}$
i.e V_{gs} ↓ ⇒ R_{ds}

Normally $V_{GS} \leq 0$ i.e '0' (or) -ve

Basic CMOS ckt :-

→ If the NMOS & PMOS transistors are connected together in a complementary, then it forms the CMOS Logic"

→ The simple CMOS ckt is shown in fig: which is used as an "Inverter". The power supply, V_{DD} typically is 2-6 V & is most often set at 5V for compatibility with TTL.



→ Ideally, the functional behaviour of CMOS can be characterised by, two cases.

→ When $V_{in} = 0V$., then N-MOS is OFF, since $V_{gs} = 0$, but, P-MOS, is ON since, it's V_{gs} is a large -ve value (-5V). Therefore Q_2 P-MOS have small resistance b/w V_{DD} & V_{out} & the O/P voltage is '5V'

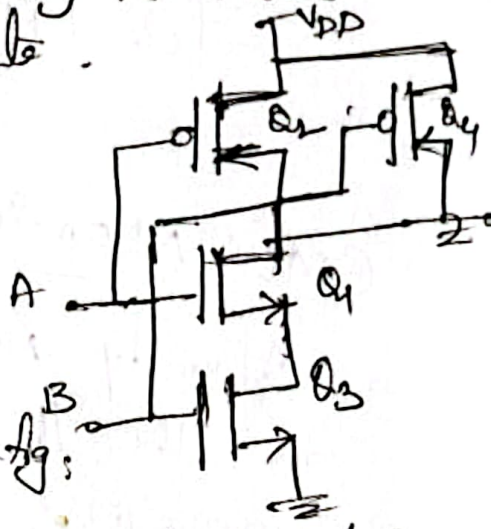
→ When $V_{in} = 5V$. then Q_1 N-MOS is ON, since it's V_{gs} is a large +ve (+5V), but, P-MOS is OFF, since it's $V_{gs} = 0$. Thus, NMOS, have small resistance b/w O/P & GND, ∴ & the O/P voltage is '0V'

→ By observing this functional behaviour it can simply act as an inverter, i.e When we are applying 0V; → O/P = 5V, & when I/P is 5V; the O/P = 0V.

CMOS NAND & NOR Gates

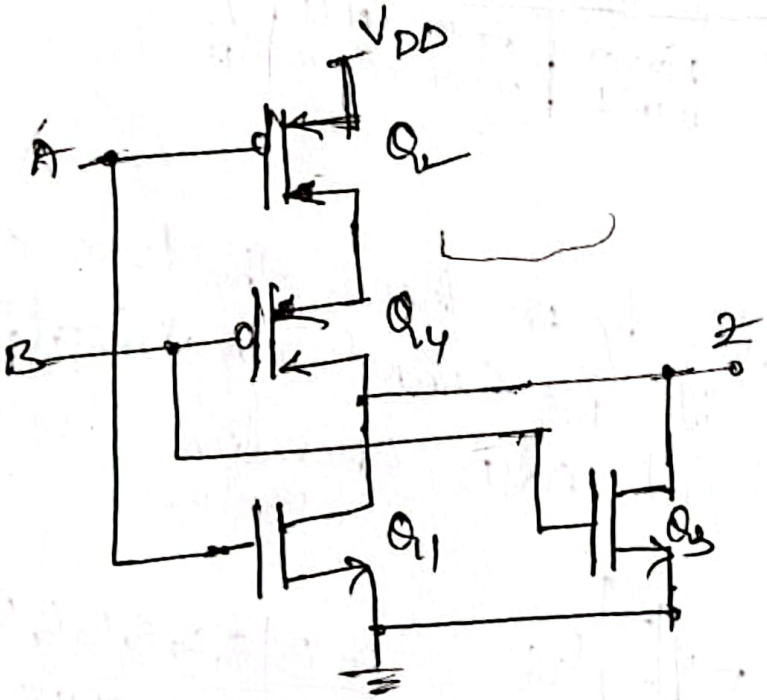
→ Both NAND & NOR Gates can be constructed using CMOS.
A 'K-I/P' Gate consists of 'K' → no. of p-MOS's
'K' → no. of 'N-MOS's'

→ The fig. shows 2-I/P CMOS NAND gate.
Generally the NAND logic is, If either of I/P is low, then O/P is high.
& If both the I/Ps are high, then the O/P is 'low', the same logic is implemented with 'CMOS' are shown in fig:



A	B	Q1	Q2	Q3	Q4	Z
0	0	OFF	ON	OFF	ON	H
0	1	OFF		OFF		H
1	0		OFF			H
1	1	OFF		OFF		L

CMOS - NOR Gate



A	B	Q1	Q2	Q3	Q4	Z
L	L	OFF		OFF		H
L	H	OFF			OFF	L
H	L		OFF	OFF		L
H	H		OFF		OFF	L

→ If both I/Ps are low, then O/P has low impedance connection to 'VDD' through p-channel MOS, & path to ground is blocked by the OFF, N-channel MOS.

→ If either I/P is High, the path to VDD is blocked, & 'Z' has low-impedance connection to GND.