UNIT-I

INTEGRATED CIRCUITS

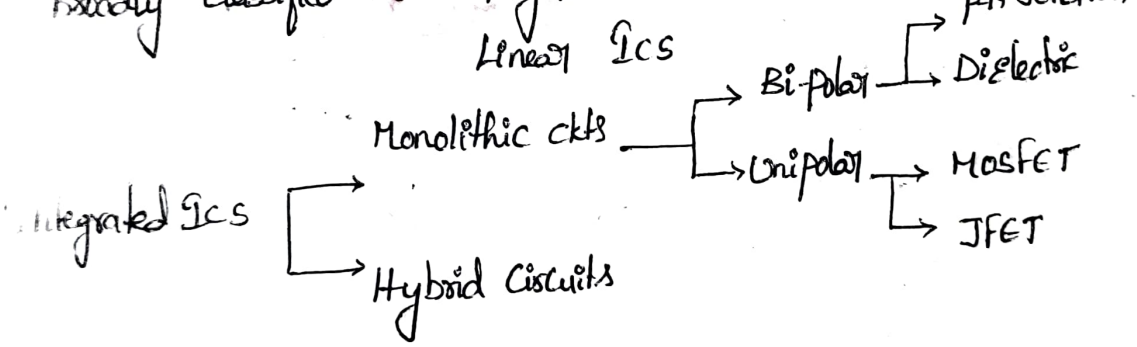
Integrated Circuit (or) IC is a miniature, low cost Electronic circuit consisting of active and passive components that are inseparably joined together on a single crystal chip of silicon.

These circuits naturally offer a no of distinct advantages

→ Miniaturization and hence increased equipment density
→ cost reduction due to batch processing
→ Increased system reliability due to elimination of soldered joints
→ Improved functional performance
→ Matched devices.
→ Increased operating speed.
→ Reduction in power consumption.

Classification of ICs

Integrated circuits offer a wide range of applications and could be broadly classified as Digital ICs
Linear ICs

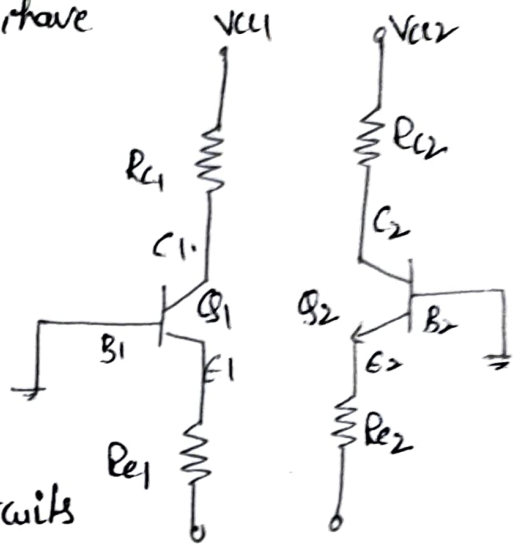


Differential Amplifier:-

A differential Amplifier forms the input stage of an operational amplifier. It is termed as "differential Amplifier" for the simple reason that it amplifies the difference of two input signals.

A differential amplifier mainly consists of two identical transistors whose emitters are directly connected as shown in fig. The d.c Power Supplies V_{CC} and V_{EE} are common to both transistors. The collector circuit resistances are equal, and the emitter resistors of the two transistors are replaced by a single resistor

Let us consider the emitter biased circuit as shown in fig.



These two emitter biased circuits have same identical characteristics i.e

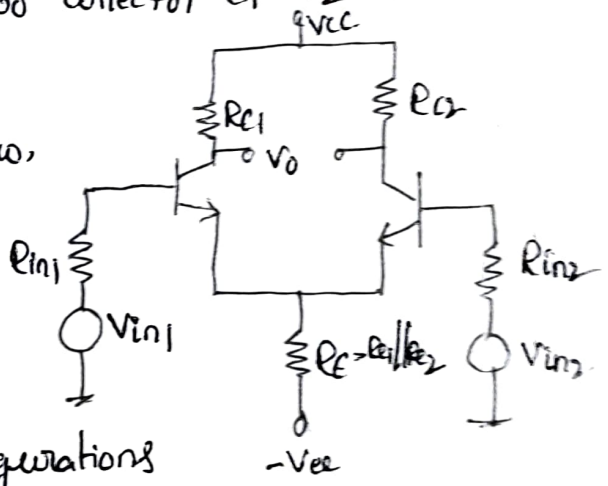
$Q_1 \& Q_2 = R_{e1} = R_{e2}$

$R_{C1} = R_{C2}$

And the magnitude of Vcc is equal to the magnitude of -Vee

→ To obtain single circuit, we should reconnect these two circuits as follows.

1. Reconnect +Vcc supply voltages of the two circuits since the voltages are of the same polarity and amp. Similarly reconnect Vee.
2. Reconnect the emitter E_1 of Q_1 to E_2 of Q_2 with Re which is $R_{E1} // R_{E2}$
3. Apply the input signal V_{in_1} to base of Q_1 and V_{in_2} to base of Q_2
4. Output is taken in between two collector C_1 & C_2 and it labled as V_o. Now the circuit is



the Differential amp of fig below, as its name implies, amp the diff b/w two inputs sigs. It is also called as diff amp

Differential amplifier Circuit Configurations

1. Dual input Balanced o/p
2. Dual input unBalanced o/p
3. Single input Balanced o/p
4. Single input unBalanced o/p

Analysis of differential Amplifier :-

The analysis of a diff amp consists in the evaluation of the circuit parameters like voltage gain, input impedece (Resistance) and output resistance. Current gain is normally defined in relation

to a diff amp, for reasons which will be Explained below.

Voltage gain

By voltage gain is meant the diff voltage gain given as $A_d = \frac{V_o}{V_{id}}$ where V_o = o/p voltage and $V_{id} = V_{i1} - V_{i2}$ the diff input voltage.

Input Resistance:- It is also termed as differential input resistance. It is the Equivalent resistance that would be measured at anyone of the input terminals, with the other terminal grounded.

It is denoted as $R_{i1} + R_{i2}$

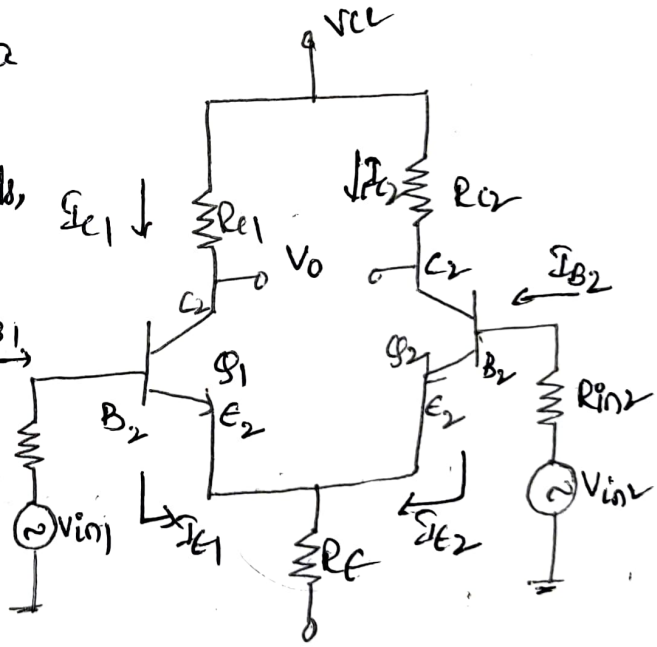
where $R_{i1} = \frac{V_{i1}}{i_{b1}}$ with $V_{i2} = 0$ & $R_{i2} = \frac{V_{i2}}{i_{b2}}$ with $V_{i1} = 0$

Output Resistance:- It is the Equivalent resistance that would be measured at either of the collector terminals w.r.t to ground.

It is denoted as R_{o1} (or) R_{o2}

Analysis of Dual input Balance o/p Mode of Diff amp:-

The circuit is shown in fig is a Dual input, balanced o/p differential amp. Notice that the two i/p signals, V_{in1} & V_{in2} are applied to the bases B_1 & B_2 of transistors Q_1 & Q_2. The o/p V_o is measured b/w the two collectors C_1 & C_2, which are at the same dc potentials.



Because of the Equal dc potential at the two collectors with respect to ground, the output is refered as a balanced output.

The Analysis of Differential amp will be in two parts

→ Dc Analysis → Ac Analysis.

DC Analysis:-

To Determine the operating point value (I_{CQ} & V_{CEQ}) for the differential amp we need (for) to obtain a dc equivalent circuit the dc equivalent circuit can be obtained simply by reducing the input signals V_{in1} & V_{in2} to zero. Now we need to determine the operating point for this the collector current I_{CQ}, V_{CEQ} must be find. Now apply KVL to base-emitter loop of transistor Q_1.

$$-R_{in} I_B - V_{BE} - R_{E_2} I_E + V_{EE} = 0$$

But $I_B = \frac{I_E}{\beta_{dc}}$ $\quad \because I_C \approx I_E$

$$-R_{in}\left(\frac{I_E}{\beta_{dc}}\right) - V_{BE} - R_{E_2} I_E + V_{EE} = 0$$

$$-R_{in}\frac{I_E}{\beta_{dc}} - R_{E_2} I_E = V_{BE} - V_{EE}$$

$$V_{EE} - V_{BE} = R_{in}\frac{I_E}{\beta_{dc}} + R_E 2 I_E$$

$$I_E\left[\frac{R_{in}}{\beta_{dc}} + 2R_E\right] = V_{EE} - V_{BE}$$

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_{in}}{\beta_{dc}} + 2R_E}$$

$$\boxed{I_E = \frac{V_{EE} - V_{BE}}{2R_E}} \quad \because 2R_E >> \frac{R_{in}}{\beta_{dc}}$$

The voltage at the emitter of Q_1 is equal to $-V_{BE}$. if we assume the voltage drop across R_{in} to be negligible small, knowing the value of emitter current $I_E \approx I_C$, we can obtain the voltage at the collector V_{cc} as follows

$$V_{cc} - I_C R_C = V_0 = V_C$$

$$V_{EC} = V_C - V_E \Rightarrow (V_{cc} - I_C R_C)(-V_{BE})$$

$$\boxed{V_{CE} = V_{cc} + V_{BE} - I_C R_C}$$

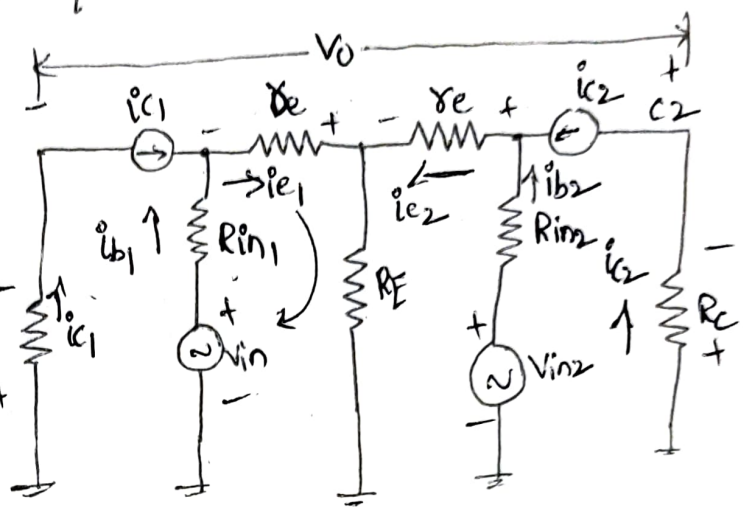
$V_{EE} - V_{BE} = 2R_C I_E + R_{in}\left[\frac{I_E}{\beta}\right]$

$V_{EE} - V_{BE} = I_E\left[2R_C + \frac{R_{in}}{\beta}\right]$

$I_C = \frac{V_{EE} - V_{BE}}{\frac{R_{in}}{\beta} + 2R_C}$

c Analysis:- To perform Ac Analysis to derive the Expression for the Voltage gain Ad, and input resistance R_i

1. Set the dc voltages V_{cc} & $-V_{EE}$ at zero.
2. Substitute small & equivalent for the transistor.



Voltage Gain:- Before we proceed to derive the Expression for the Voltage Gain Ad, the following should be noted about the circuit in fig.

1. $I_{E_1} = I_{E_2}$, therefore $r_{e_1} = r_{e_2}$; for this reason, the ac emitter resistance of transistor Q_1 and Q_2 is simply denoted by r_e.
2. The voltage across each collector resistor is shown out of phase by 180° w.r.t to the i/p voltages V_{in_1} and V_{in_2}. This polarity assignment is in accordance with the common emitter config. As we have seen, the diff amp is basically constructed in a CE config using two identical CE circuits.
3. Note the assigned polarity of the o/p voltage V_o this polarity simply indicates that the voltage at collector C_2 is assumed to be more +ve w.r.t to ground.

Apply KVL for Loop I & II

$$V_{in_1} - R_{in_1} I_{b_1} - r_e i_{e_1} - R_E (i_{e_1} + i_{e_2}) = 0 \quad \text{——— (1)}$$

$$V_{in_2} - R_{in_2} I_{b_2} - r_e i_{e_2} - R_E (i_{e_1} + i_{e_2}) = 0 \quad \text{——— (2)}$$

sub current Relations $i_{b_1} = i_{e_1}/\beta_{ac}$ and $i_{b_2} = i_{e_2}/\beta_{ac}$ yields

$$V_{in_1} - \frac{R_{in_1}}{\beta_{ac}} i_{e_1} - r_e i_{e_1} - R_E (i_{e_1} + i_{e_2}) = 0 \quad \text{——— (3)}$$

$$V_{in_2} - \frac{R_{in_2}}{\beta_{ac}} i_{e_2} - r_e i_{e_2} - R_E (i_{e_1} + i_{e_2}) = 0 \quad \text{——— (4)}$$

$R_{in_1} \| R_{ac} + R_{in_2} \| R_{ac}$ very small values so we can neglect the values

$$(r_e + R_E) i_{e_1} + (R_E) i_{e_2} = V_{in_1}$$
$$(R_E) i_{e_1} + (r_e + R_E) i_{e_2} = V_{in_2}$$

By using Cramer's rule

$$i_{e_1} = \frac{\begin{vmatrix} V_{in_1} & R_E \\ V_{in_2} & r_e + R_E \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$= \frac{(r_e + R_E) V_{in_1} - (R_E) V_{in_2}}{(r_e + R_E)^2 - (R_E)^2} \quad \text{---(5)}$$

By $i_{e_2} = \dfrac{\begin{vmatrix} r_e + R_E & V_{in_1} \\ R_E & V_{in_2} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}} = \dfrac{(r_e + R_E) V_{in_2} - (R_E) V_{in_1}}{(r_e + R_E)^2 - (R_E)^2}$ ---(6)

The output voltage is $V_o = V_{c_2} - V_{c_1}$

$$= -R_c i_{c_2} - (-R_c i_{c_1})$$
$$= R_c i_{c_1} - R_c i_{c_2}$$
$$= R_c [i_{c_1} - i_{c_2}] \quad \because i_c \approx i_e$$
$$= R_c [i_{e_1} - i_{e_2}]$$

Now sub i_{e_1} & i_{e_2}

$$V_o = R_c \left[\frac{(r_e + R_E) V_{in_1} - (R_E) V_{in_2}}{(r_e + R_E)^2 - (R_E)^2} - \frac{(r_e + R_E) V_{in_2} - (R_E) V_{in_1}}{(r_e + R_E)^2 - (R_E)^2} \right]$$

$$= R_c \left[\frac{(r_e + R_E)(V_{in_1} - V_{in_2}) + (R_E)(V_{in_1} - V_{in_2})}{(r_e + R_E)^2 - (R_E)^2} \right]$$

$$= R_C \left[\frac{(V_{in_1} - V_{in_2})[r_e + 2R_E]}{r_e^2 + R_E^2 + 2r_e R_E - R_E^2} \right]$$

$$= R_C \left[\frac{(r_e + 2R_E)(V_{in_1} - V_{in_2})}{r_e^2 + 2r_e R_E} \right]$$

$$= R_C \left[\frac{(r_e + 2R_E)(V_{in_1} - V_{in_2})}{r_e[r_e + 2R_E)} \right]$$

$$V_o = R_C \left[\frac{V_{in_1} - V_{in_2}}{r_e} \right]$$

Thus a diff amp amplifies the diff b/w two input signals $V_{id} = V_{in_1} - V_{in_2}$ and o/p is

$$\boxed{V_o = \frac{R_C}{r_e} \left[V_{in_1} - V_{in_2} \right]}$$

$$A_d = \frac{V_o}{V_{id}} = \frac{\frac{R_C}{r_e}\left[V_{in_1} - V_{in_2} \right]}{V_{id}}$$

$$\boxed{A_d = \frac{R_C}{r_e}}$$

Differential amplifier input Resistance :- Diff i/p Resistance is defined as the equivalent resistance that would be measured at either i/p terminal with other terminal grounded. this means that the input resistance R_i, seen from the i/p signal source V_{in_1} is determined with the signal source V_{in_2} set at zero. Similary, the i/p signal source V_{in_1} is set at zero to determine the i/p resistance R_{i2} seen from the i/p signal source V_{in_2}. Usually the source resistance R_{in_1} & R_{in_2} are very small and hence will be ignored in the derivation of input resistance R_i & R_{i2}

$$R_{i_1} = \left| \frac{V_{in1}}{i_{b1}} \right|_{V_{in2}=0}$$

$$\left| \frac{V_{in1}}{i_{e1}} \right|_{\beta_{ac}} \Big|_{V_{in2}=0}$$

Sub the value of i_{e1} from equation (5) we get

$$R_{i_1} = \frac{\beta_{ac} V_{in1}}{(r_e + R_E) V_{in1} - (R_E)_0} = \frac{\beta_{ac}(r_e^2 + 2R_e r_e)}{(r_e + R_E)} = \frac{\beta r_e (r_e + 2R_e)}{r_e + R_E}$$

$$= \frac{\beta r_e (2R_{eq})}{R_E}$$

$$R_{i_1} = \frac{\beta_{ac} r_e (2R_E)}{R_E}$$

(∵ $r_e \ll R_E$ so that $r_e + 2R_E = 2R_E$)

$$\boxed{R_{in1} = 2 r_e \beta_{ac}}$$

$$R_{in1} = \left| \frac{V_{in1}}{i_{b1}} \right|_{V_{in2}=\infty}$$

$$\frac{\beta V_{in1}}{i_{e1}} \quad \frac{r_e^2 + R_E^2 + 2r_e R_E}{r_e + R_E}$$

$$\frac{\beta V_{in1}}{(r_e + R_E) V_{in} - R_E V_{in}} \quad \frac{r_e + R_E}{(r_e + R_E) - R_E}$$

$$\frac{\beta (r_e + R_E)^2 - R_E^2}{(r_e + R_E) - R_E}$$

Parally input resistance $R_{i2} = \left| \frac{V_{in2}}{i_{b2}} \right|_{V_{in1}=0}$

$$= \left| \frac{V_{in2}}{i_{e2}} \right|_{\beta_{ac}} \Big|_{V_{in1}=0}$$

$$\boxed{R_{i2} = 2\beta_{ac} r_e}$$

output resistance :- output resistance defined as the equivalent resistance that would be measured at either o/p terminal w.r to ground

$$R_{O1} = R_{O2} = R_C$$

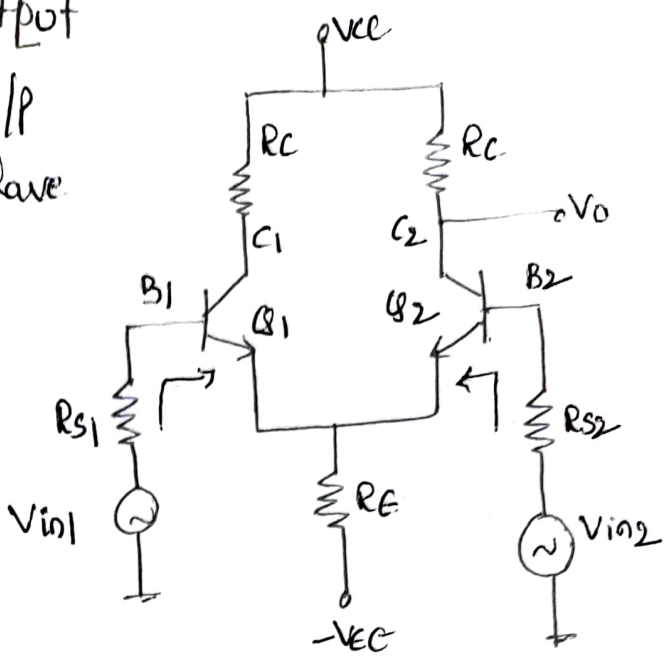
The Current gain of the diff-amp is undefined.

$$V_0 = R_C [i_{e1} - i_{e2}]$$

$$V_0 = \left[\frac{(r_e + R_E) V_{in1} - R_E (V_{in2})}{(r_e + R_E)^2 - R_E^2} \right] - \left[\frac{(r_e + R_E) V_{in2} + R_E V_{in1}}{(r_e + R_E)^2 - R_E^2} \right]$$

$$V_0 = \frac{r_e + R_E [V_{in1} - V_{in2}] + R_E [V_{in1} - V_{in2}]}{(r_e + R_E)^2 - R_E^2}$$

Dual input unBalanced output



For Dual input unBalanced o/p differential Configuration also have as same as analysis like Dual i/p Balance o/p.

For DC Analysis the Q-point are I_{CQ} & V_{CEQ}.

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C$$

* The Resistence $R_{i1} = R_{i2} = 2\beta_{ac} r_e$ as same as Dual i/p Balance o/p.
* The o/p Resistence is $R_{o1} = R_C$.

For Ac Analysis

$$V_o = V_{C2}$$
$$= -R_C i_{C2}$$

Diff o/p $V_o = -R_C i_{e2}$

$$V_o = R_C \left[\frac{(r_e + R_E) V_{in2} - (R_E) V_{in1}}{(r_e + R_E)^2 - (R_E)^2} \right]$$

$$= R_C \left[\frac{r_e V_{in2} + R_E [V_{in2} - V_{in1}]}{r_e^2 + R_E^2 + 2 r_e R_E - R_E^2} \right] = \frac{V_{in2}(r_e + R_E) - R_E V_{in1}}{}$$

$$R_C \left[\frac{r_e V_{in2} + R_E [V_{id}]}{r_e^2 + 2 r_e R_E} \right]$$ let $r_e V_{in2} \ll R_E V_{id}$ & $r_e^2 \ll 2 r_e R_E$

Then $R_C \left[\frac{R_E V_{id}}{2 r_e R_E} \right]$

$$V_o = \frac{R_C}{2 r_e} (V_{id})$$

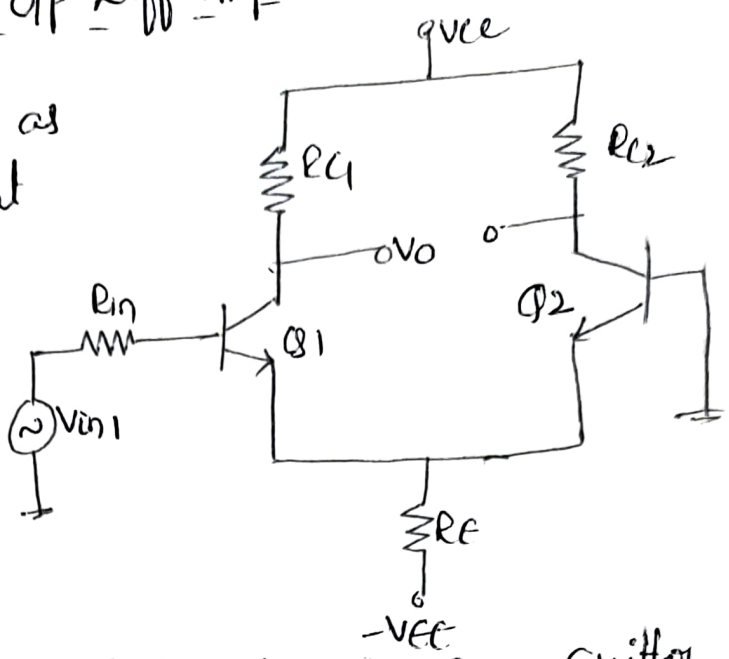
The Gain $\frac{V_o}{V_{id}} = \frac{R_C}{2 r_e}$

③ Single input Balanced o/p Diff Amp:-

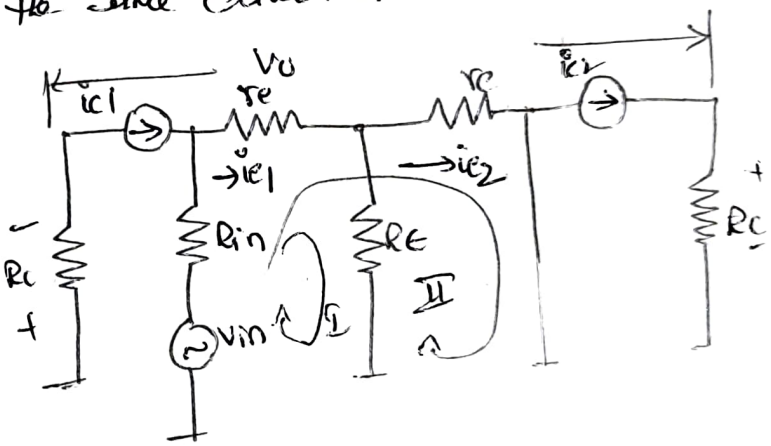
The Dc Analysis is as same as dual i/p Bal mode. So that the Q point are

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + R_{in}/\beta_{dc}}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$



Ac Analysis:- During the +ve half cycle. The Base Emitter jn of Q_1 is +ve and that of Q_2 is -ve, so that I_{C_1} increases, I_{e_2} decreases from the operating point value I_{CQ} This change collector current (gives same direction) shown in fig. in which the current of both i_{c_1} and i_{c_2} are shown to be in the same direction.



Apply KVL for loop ① and ②

$$V_{in} - i_{b_1}R_{in} - r_e i_{e_1} - I_E R_E = 0 \quad \text{—①}$$

$$V_{in} - i_{b_1}R_{in} - r_e i_{e_1} - r_e i_{e_2} = 0 \quad \text{—②}$$

$$I_E = (i_{e_1} - i_{e_2}) \qquad i_{b_1} = \frac{R_{in} i_{e_1}}{\beta_{ac}}$$

Sub the

$$V_{in} - \frac{R_{in} i_{e_1}}{\beta_{ac}} - r_e i_{e_1} - R_E i_{e_1} + R_E i_{e_2} = 0 \quad \text{——③}$$

$$V_{in} - \frac{R_{in} i_{e_1}}{\beta_{ac}} - r_e i_{e_1} - r_e i_{e_2} = 0 \quad \text{——④}$$

$$V_{in} = r_e i_{e_1} + R_E i_{e_1} - R_E i_{e_2}$$

$$V_{in} = r_e i_{e_1} + r_e i_{e_2}$$

So that we can write these Vin

$V_{in} = i_{e_1}(r_e + R_E) - i_{e_2} R_E$ ——— (5)

$V_{in} = i_{e_1} r_e + i_{e_2} r_e$ ——— (6)

Apply Cramer's rule

$$i_{c_1} = \frac{\begin{vmatrix} V_{in} & -R_E \\ V_{in} & r_e \end{vmatrix}}{\begin{vmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{vmatrix}} = \frac{r_e V_{in} + R_E V_{in}}{r_e(r_e + R_E) + r_e R_E}$$

$$= \frac{V_{in}(r_e + R_E)}{r_e(r_e + 2R_E)} \quad \text{——— (7)}$$

$$i_{e_2} = \frac{\begin{vmatrix} (r_e + R_E) & V_{in} \\ r_e & V_{in} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{vmatrix}} = \frac{V_{in}(r_e + R_E) - V_{in} r_e}{r_e(r_e + R_E) + r_e R_E} = \frac{V_{in}[\cancel{r_e} + R_E - \cancel{r_e}]}{r_e[r_e + 2R_E}$$

$$= \frac{V_{in} R_E}{r_e[r_e + 2R_E]} \quad \text{——— (8)}$$

Now the Parameters are

output voltage $V_0 = V_{c_2} - V_{c_1}$

$= R_c i_{c_2} - (-R_c i_{c_1})$

$R_c[i_{c_2} + i_{c_1}]$

$R_E[i_{c_2} + i_{e_1}]$

$$= R_c \left[\frac{V_{in} R_E}{r_e(r_e + 2R_E)} + \frac{V_{in}(r_e + R_E)}{r_e(r_e + 2R_E)} \right]$$

$$= R_c \left[\frac{V_{in}[R_E + r_e + \cancel{R_E}]}{r_e(r_e + 2R_E)} \right]$$

$$V_0 = R_E \left[\frac{V_{in}}{r_e} \right]$$

$$V_o = \frac{R_c V_{in}}{r_e}$$

Differential Voltage Gain :- $\frac{V_o}{V_i^o} = \frac{R_c V_{in}}{r_e} \Big/ V_{in}$

$$A_{vd} = \frac{V_o}{V_i^o} = \frac{R_c}{r_e}$$

Differential Input Resistance :-

$$R_{in_1} = \left| \frac{V_{in_1}}{i_{b_1}} \right|_{V_{in_2}=0}$$

$$R_{in} = \frac{V_{in}}{i_{e_1}/\beta_{ac}} = \frac{V_{in}\beta_{ac}}{i_{e_1}}$$

$$R_{in} = \frac{V_{in}\beta_{ac}}{V_{in}[r_e+2R_E)} = \frac{\beta_{ac} r_e (r_e+2R_E)}{r_e + 2R_E} \quad \text{if } r_e \ll R_E$$

$$r_e [r_e+2R_E]$$

$$R_{in} = \frac{\beta_{ac} 2R_E r_e}{R_E} = 2\beta_{ac} r_e$$

$$R_{in_1} = 2\beta_{ac} r_e$$

Differential out Resistance $R_{o_1} = R_{o_2} = R_C$

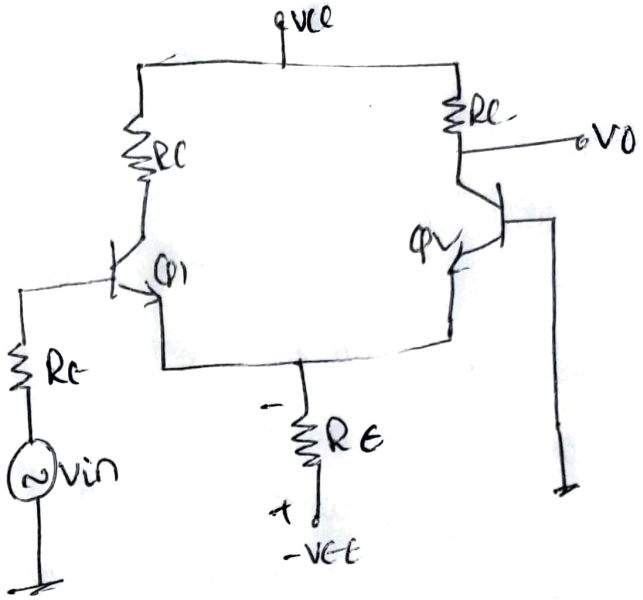
(4) Single input un Balanced output

The properties of single input unBalanced output is same as single input Balanced output the DC analysis of this configuration is

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + R_{in}/\beta_{dc}}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

Analysis



$V_o = R_c i_{c1}$

$$V_o = R_c \left[\frac{V_{in} (r_e + R_E)}{r_e (r_e + 2R_E)} \right]$$

$$V_o = R_c \left[\frac{V_{in} R_E}{r_e (2R_E)} \right] \quad r_e \ll R_E \text{ or } r_e \ll 2R_E$$

$$V_o = \frac{R_c}{2r_e} V_{in}$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{R_c}{2r_e}}$$ Ad Voltage Gain.

Block Diagram of Operational Amp:-

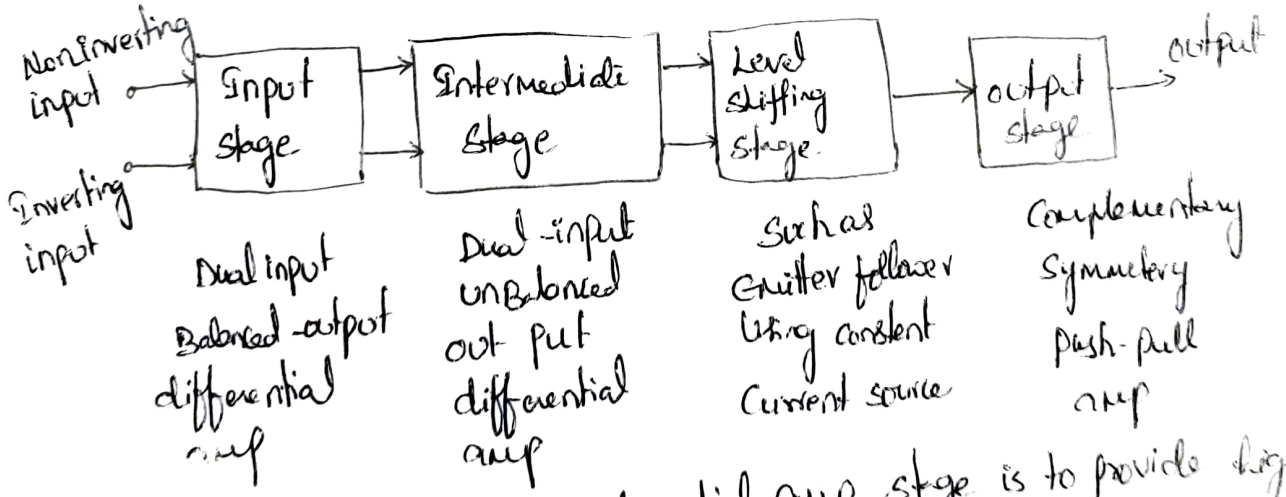
→ Commercial IC op-Amp usually consists of four cascaded blocks as shown in fig. The first two stages are cascaded differential amplifiers and are designed to provide high gain and High input impedance.

→ The third stage acts as a buffer as well as a level shifter. The buffer is usually an Emitter follower whose input impedance is very high so that it prevents loading of the high gain stage.

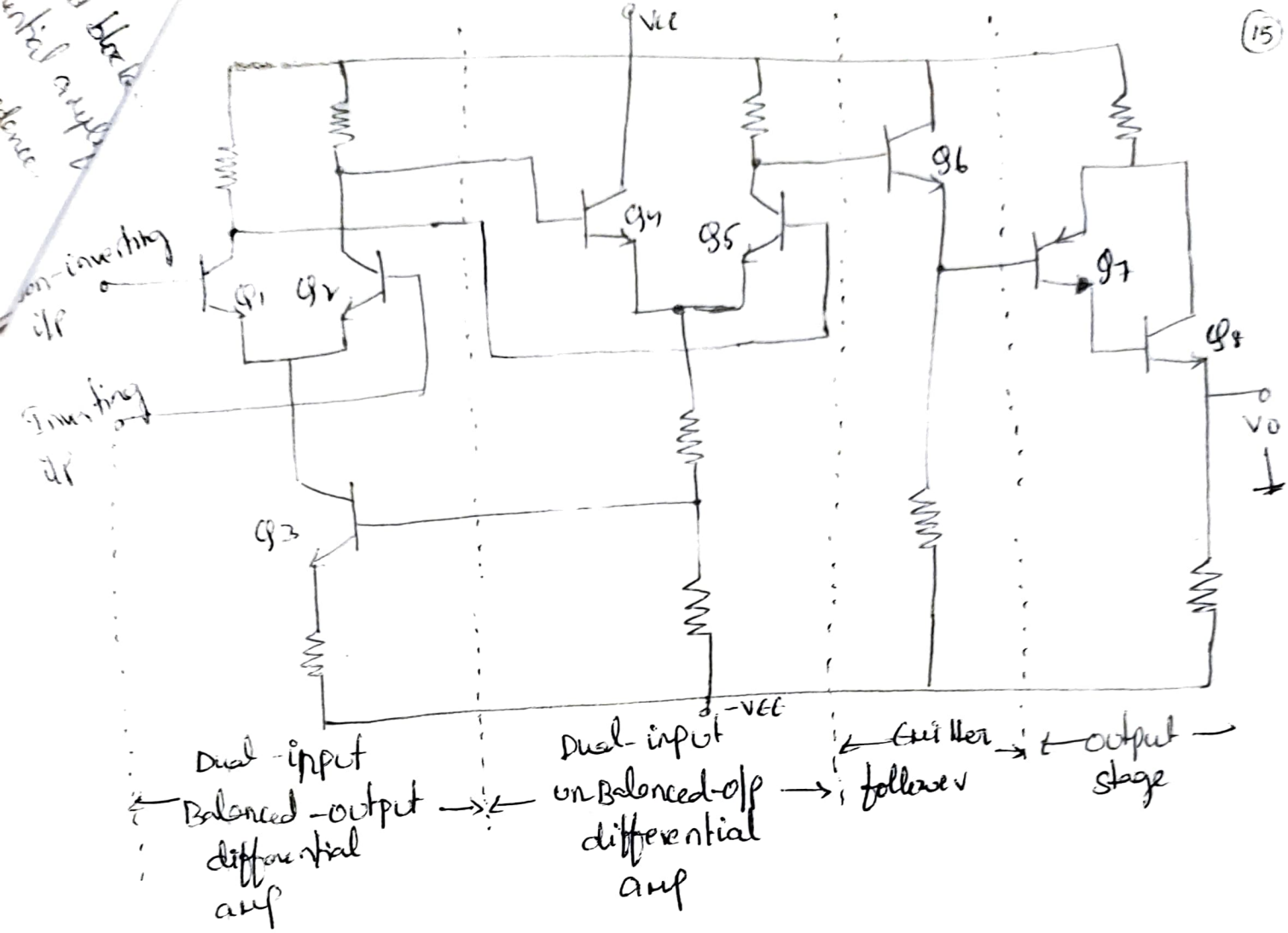
→ The level shifter adjusts the dc voltages, so that output voltage is zero for zero inputs.

→ The adjustment of d.c level is required as the gain stages are direct coupled. As it is not possible to fabricate large value of capacitor, all IC's are direct coupled usually.

→ The output voltage should swing symmetrically with respect to ground to allow such symmetrical swing, the amplifier is provided with both positive and negative supply voltages. Power supply voltages of ±15V are common.



The main purpose of the differential amp stage is to provide high gain to the difference mode signal and cancel the common-mode signal. Thus, it is able to suppress any undesired noise which is common to both of the input terminals.



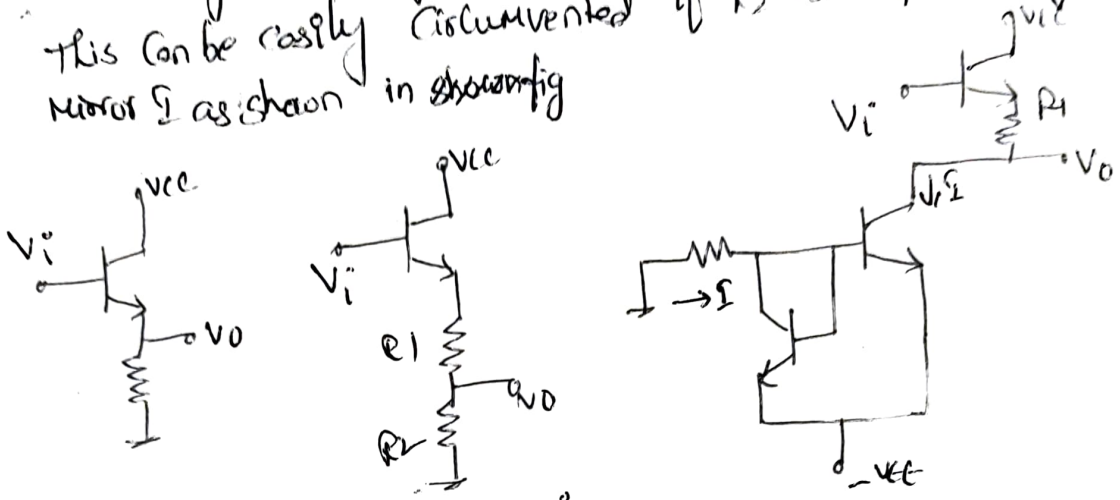
Level Translator:-

There are two good reasons for using a level shifter in an Op-Amp. As we want an op-amp to operate down to dc, no coupling capacitor is used. Because of direct coupling, the dc level rises from stage to stage. The increase in dc level tends to shift the operating point of the next stage. This, in turn, limits the output voltage swing and may even distort the output signal. It, therefore, becomes essential that the equiescent voltage of one stage is shifted, before it is applied to the next stage. Another requirement to be satisfied is that the output should have quiescent voltage level of 0V for zero input signal.

The simplest type of a level shifter is shown in fig. It may be noted that this is basically an Emitter follower. Hence the level shifter also acts as a buffer to isolate the High gain stages from the output stage. The amount of shift obtained

$$V_o - V_i = -V_{BE} \simeq -0.7\,V$$

If this shift is insufficient the output can be taken at the junction of two resistors R_1 and R_2. The voltage shift is now increased by the drop across R_1. However, this arrangement has the disadvantage that signal voltage also gets attenuated by $R_2/(R_1+R_2)$. This can be easily circumvented if R_2 is replaced by a current mirror I as shown in fig



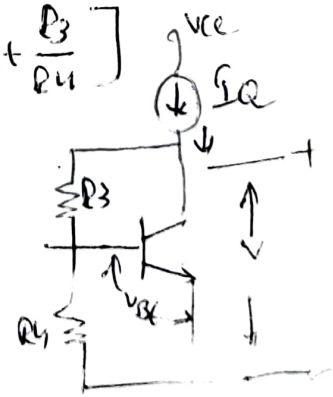
the shift in level now is

$$V_o - V_i = -(V_{BE} + IR_1)$$

and there is no ac attenuation due to high resistance of the current source.

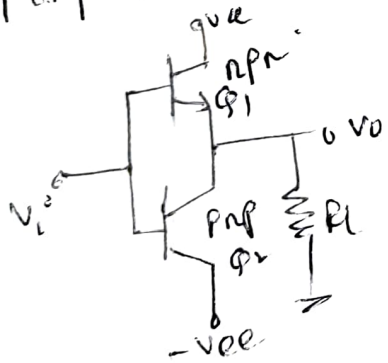
Another voltage source commonly used in μA741 opamp is shown in fig. It can be seen that if base current is negligible compared to the current in R_3 and R_4, then the circuit behaves as a V_{BE} multiplier as

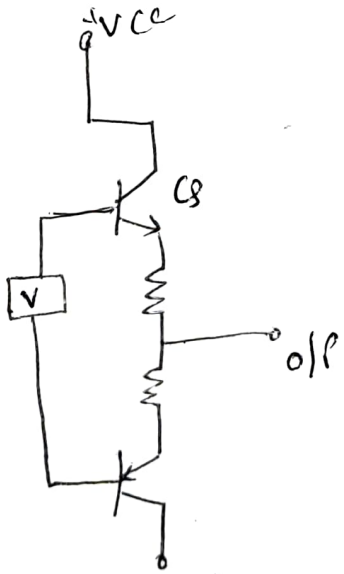
$$V = \frac{V_{BE}}{R_4}(R_3+R_4) = V_{BE}\left[1+\frac{R_3}{R_4}\right]$$



This voltage source can be used to replace R_1 in shown in fig

The function of the last stage, that is the o/p stage in an op-amp is to supply the load current and provide a low impedance o/p. It should also provide a large output voltage swing, ideally the total supply voltage ie $V_{cc} + V_{ee}$. A simple o/p stage consists of two complimentary transistors Q_1 (npn) and Q_2 (pnp) connected as emitter followers as show in fig. It can be seen that for V_i positive, transistor Q_1 is on and supplies current to load R_L. And if V_i is negative, Q_1 is cut off and Q_2 acts as a sink to remove current from the load R_L. There is, however, a limitation in this circuit. The o/p voltage V_o remains zero until the input V_i exceeds V_{BE} (cut-in) = 0.5 V this is called crossover distortion. It can be eliminated by applying a bias voltage V slightly greater than $2V_{BE} = 1V$ between the two bases, so that small current flows in the transistors even in the quiescent state. The o/p stage of μA741 op amp is shown in fig





Current Mirror:- (Constant Current Source)

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage. In the basic circuit, transistors Q_1 and Q_2 are matched as the circuit is fabricated using IC technology.

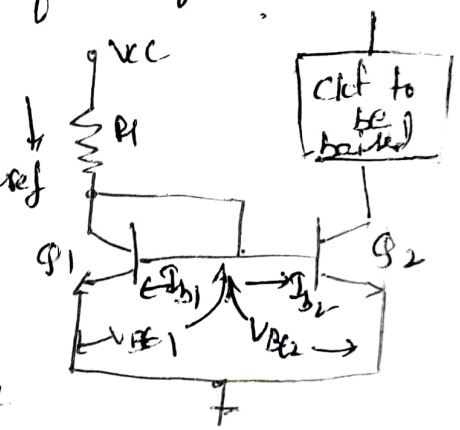
It may be noted that bases and emitter of Q_1 and Q_2 are tied together and thus have the same V_{BE}, In addition, transistor Q_1 is connected as a diode by shorting its collector to base

The i/p current I_{ref} flows through the diode connected transistor Q_1 and thus establishes a voltage across Q_1, This voltage in turn appears between the base and emitter of Q_2. Since Q_2 is identical to Q_1, the emitter current of Q_2 will be equal to emitter current of Q_1 which is approximately equal to I_{ref}.

Thus, we can say that as long as Q_2 is maintained in the active region, its collector current $I_{C_2} = I_o$ will be approximately equal to I_{ref}.

Since the output current I_o is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

This mirror effect is however, valid only for large value of β. To study the effect of β on the operation of the current mirror circuit, we analyze it further



Analysis

The collector current I_{C_1} and I_{C_2} for transistors Q_1 and Q_2 can be approximately expressed as

$$I_{C_1} = \alpha_f I_{ES} e^{V_{BE1}/V_T}$$

$$I_{C_2} = \alpha_f I_{ES} e^{V_{BE2}/V_T}$$

These two equation may write

$$\frac{I_o}{I_{C1}} = e^{(V_{BE2} - V_{BE1})/V_T}$$

$V_{BE1} = V_{BE2}$

$I_{C2} = I_{C1} = I_C = I_o$

Also since both the transistors are identical $\beta_1 = \beta_2 = \beta$

KCL at the collector of Q_1 gives

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2} = I_C\left[1 + \frac{2}{\beta}\right]$$

I_C may be expressed as

$$I_C = \frac{\beta}{\beta+2} I_{ref}$$

where I_{ref} can be seen to be (from fig)

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} \quad (\text{as } V_{BE} \approx 0.7V)$$

for $\beta \gg 1$, $\beta/(\beta+2)$ is almost unity and the output current I_o is equal to the ref current, I_{ref} which for a given R_1 is constant. Typically I_o varied by about 3% for $50 \le \beta \le 200$.

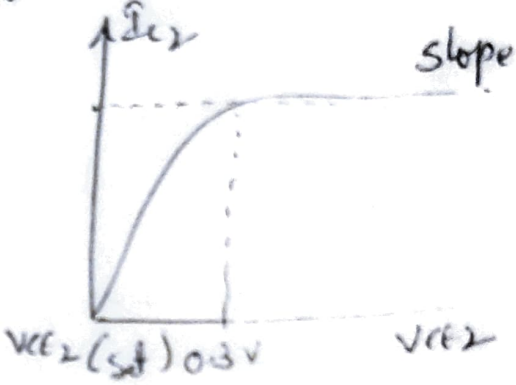
It is possible to obtain current transfer ratio other than unity simply by controlling the area of the emitter-base junction of the transistor Q_2. For example, if the area of EBJ of Q_2 is 4 times that of Q_1, then $I_o = 4 I_{ref}$

the o/p resistance of the current source is the o/p resistance r_{o2} of Q_2

$$R_o = r_{o2} = \frac{V_A}{I_o} \simeq \frac{V_A}{I_{ref}} \quad [V_A \text{ is the early voltage}]$$

the circuit however operates as a constant current source as long as Q_2 remain in the active region. From the V-A characteristics of Q_2 as shown in fig, it can be seen that for $V_{CE2} < 0.3V$, Q_2 is saturated. For $V_{CE2} > 0.3V$ transistor operates in the active region and I_o

is essentially constant the slight increase in I_{C_2} is due to Early effect. The 1/slope of the curve in this region gives the o/p resistance r_o of the current source for all practical purposes, early voltage may be assumed to be infinite, so that $r_o \to \infty$ and I_{C_2} is constant



Analysis requiring small signal Analysis of Differential Amplifier:-

→ An ideal dual input, balanced o/p differential amplifier as shown in fig. should amplify only the differential signal at the two inputs and reject the signal common to these inputs

→ As transistors Q_1 and Q_2 are a matched pair of transistors, thus any unwanted signal, such as noise (or) hum pick up which is common to both the inputs would get rejected.

→ However in a practical case transistors Q_1 and Q_2 are not Equally matched and output does appear even when same voltage is applied to the two i/p terminals.

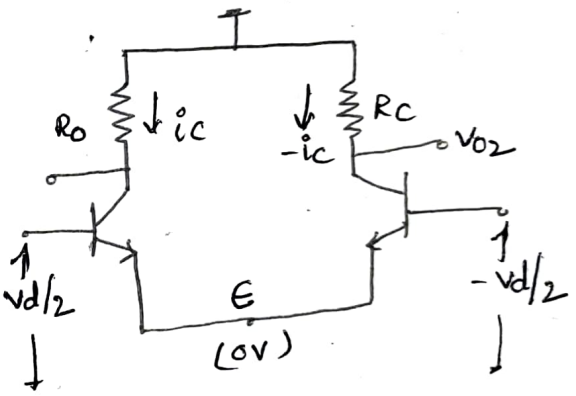
→ Due to this here we have to Compute the small signal differential mode gain, A_{DM} and Common-Mode gain A_{CM}.

→ These Expressions help in finding the fig of CMRR.

Differential-Mode Gain, A_{DM}:-

→ for $v_1 = v_2$, the current I_Q divides Equally into the two transistors Q_1 & Q_2 because of the symmetry of ckt.

→ However, if v_1 is now increased by an incremental voltage $v_d/2$ and v_2 is decreased by $v_d/2$.



→ The Common mode small signal is naturally zero.

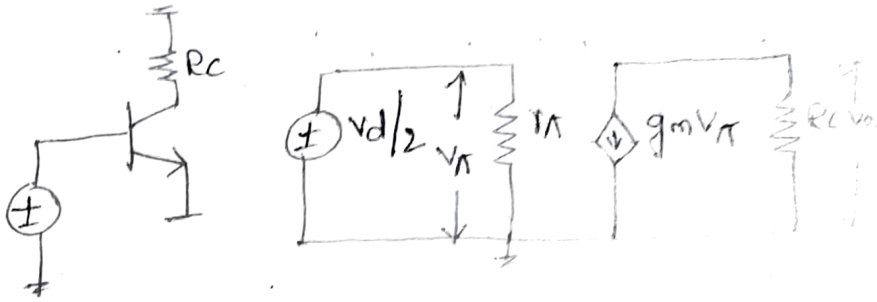
→ The Collector Current i_{c1} will now increase by i_c and i_{c2} will decrease by Equal amount

→ The sum of total Currents in transistors Q_1 & Q_2 however remains constant as Contrained by the constant current I_Q. As there is no change in of Current through R_E, V_E at ϵ remains Constant.

→ The below fig shows the small signal Equivalent of differential amplifier.

Analysis Using Hybrid-π Model:-

Since the performance of two sides of the differential amp is identical, we need to analyze only one side of the differential amp called differential half circuit. The fig shows the single stage CE transistor amp fed by a small signal voltage $V_d/2$ and its a.c equivalent circuit using Hybrid-π model.



The Gain at V_{o_1} is

$$V_{o_1} = -g_m R_c V_\pi$$

$$\frac{V_{o1}}{V_\pi} = -g_m R_c \quad \because V_d/2 \simeq V_\pi$$

$$\frac{V_{o1}}{V_d/2} = -g_m R_c \longrightarrow \boxed{\frac{V_{o1}}{V_d} = \frac{1}{2} g_m R_c}$$

$$\text{//ly} \quad \frac{V_{o2}}{V_d/2} = -g_m R_c \longrightarrow \boxed{\frac{V_{o2}}{V_d} = +\frac{1}{2} g_m R_c}$$

The output voltage signal of a differential amplifier can be taken either differentially or single-ended. If the o/p is taken differentially then, the differential-mode gain, A_{DM} is given by

$$A_{DM} = \frac{V_{o1} - V_{o2}}{V_d} = -g_m R_c \quad (\text{Differential mode})$$

On the other hand, if o/p is single-ended, then the differential mode gain A_{DM} is given by

$$A_{DM} = \frac{V_{o1}}{V_d} = -\frac{1}{2} g_m R_c$$

$$= \frac{V_{o2}}{V_d} = \frac{1}{2} g_m R_c.$$

In the above analysis, we have not included the o/p resistance

UNIT: II

Characteristics of Op-Amp

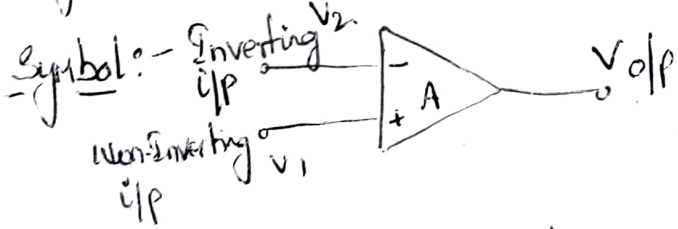
Operational Amplifier:-

An operational amplifier is a direct-coupled high gain amplifier usually consisting of one or more different amplifiers and usually followed by a level translator and an output stage is generally a pushpull or push-pull complementary-symmetry pair. An operational amplifier is available as a single integrated circuit package.

The operational amp is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for performing mathematical operations such as addition, subtraction, multiplication, and integration.

Thus the name operational amplifier stems from its original use for these mathematical operations and is abbreviated to op-amp. With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications, such as ac and dc signal amplification, active filters, oscillators, comparators, regulators and others.

Symbol:-



Types of Integrated Circuits:-

Integrated circuits may be classified as either → Monolithic
→ Hybrid

Most linear ICs are produced by the monolithic process in that all transistors and passive elements are fabricated on a single piece of semiconductor material, usually silicon.

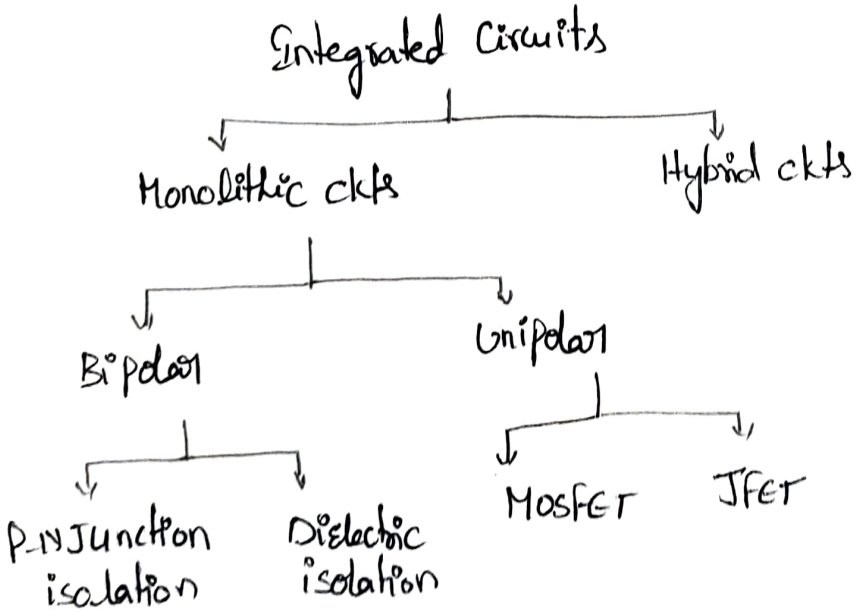
Monolithic is a Greek-based word meaning one stone

In Monolithic ICs all components are formed simultaneously by a diffusion process. Then a metallization process is used in interconnecting these components to form the desired circuit. Electrical isolation between the components in monolithic ICs can be achieved by any one of three isolation techniques:- dielectric, beam-lead (or) PN Junction

In Hybrid ICs, passive components and the interconnections between them are formed on an insulating substrate. The sub-strate is used as a chassis for the integrated components. Active components such as transistors, and diodes, as well as monolithic integrated circuits are then connected to form a complete circuit. For this reason, low volume production methods are best suited to hybrid IC technology.

Classification :-

- Digital ICs
- Linear ICs



Fabrication of typical Circuit:-

They are many steps utilized to converting the circuit into Integrated IC.

1 Silicon wafer (substrate) preparation
2 Epitaxial growth
3 Oxidation
4 photolithography
5 Diffusion
6 Ion implantation
7 Isolation techniques
8 Metallization
9 Assembly processing and packaging.

Packages of IC :- there are three popular packages available :-

1. The metal can (TO) package
2. The dual-in-line package (DIP)
3. The flat package (or) flat pack

op-amp packages may contain single, two (dual) or four (quad) op-amps. Typical package have 8 terminals, 10 terminals and 14 terminals The widely used a very popular type, for exp μA 741 is a single op-amp and is available as an 8 pin can, an 8-pin DIP, a 10-pin flat package (or) a 14-pin DIP. The μA 747 is a dual 741 and comes in either a 10 pin can (or) a 14-pin package.

op-amp terminals :- opamp have five basic terminals, ie two input terminals, one output terminal and power supply terminals. The significance of other terminals varies with the type of op-amp.

Refer the following figs (a), Top view of a metal can package. It has 8 pins with no 8 identified by a tab. other pins are numbered clockwise fourm pin8, begining with PIN 1.

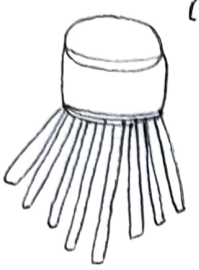
PIN 2 is called the inverting input terminal and PIN 3 is Non-inverting i/p terminal

PIN 6 is output terminal and PIN 7 & 4 are power supply terminals labled as V^+ and V^- respectively. Terminals 1 and 5 are used for dc offset. The pin 8 marked NC indicates No Connection.

In the case of Dip package of 741 as shown in fig b & c.

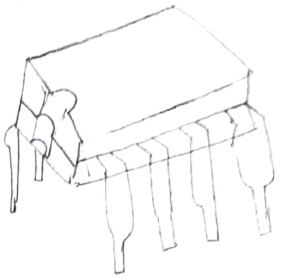
The top pin on the left of the notch locates pin 1.

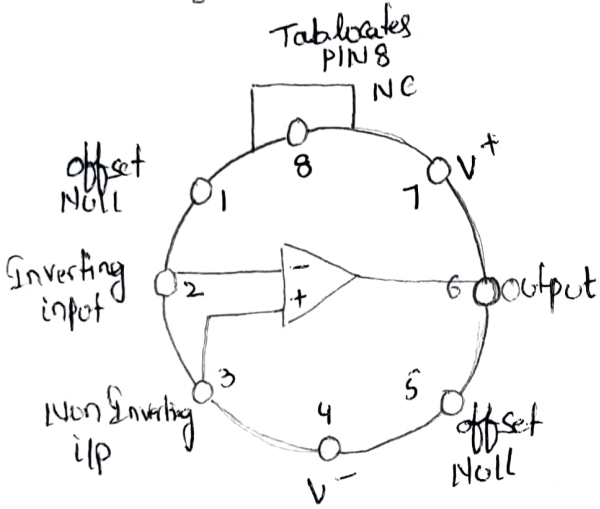
The other case is flatpack as shown in fig (d)



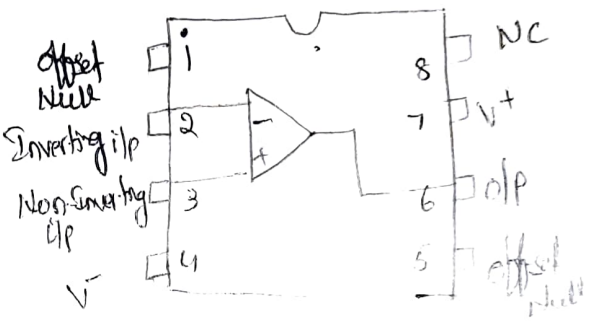
TO-5 style package with straight leads

Dual in-line plastic package



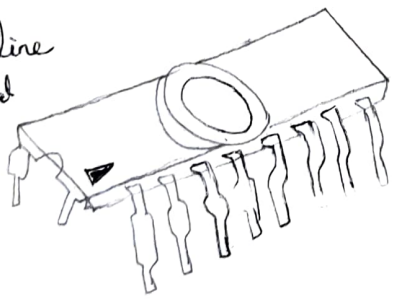


(a) 8-pin Metal can

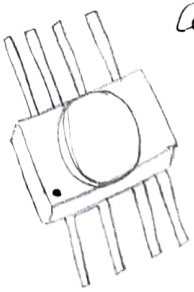


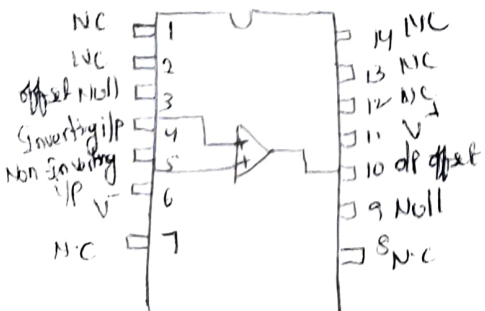
(b) 8-pin Mini Dip

Dual in-line welded seal ceramic Package

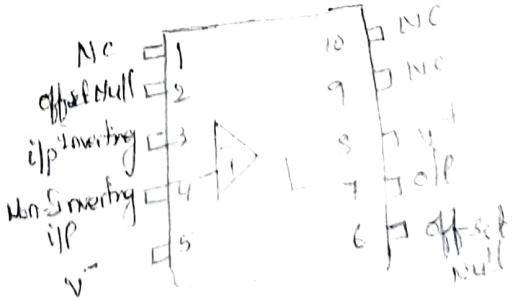


Ceramic flat package





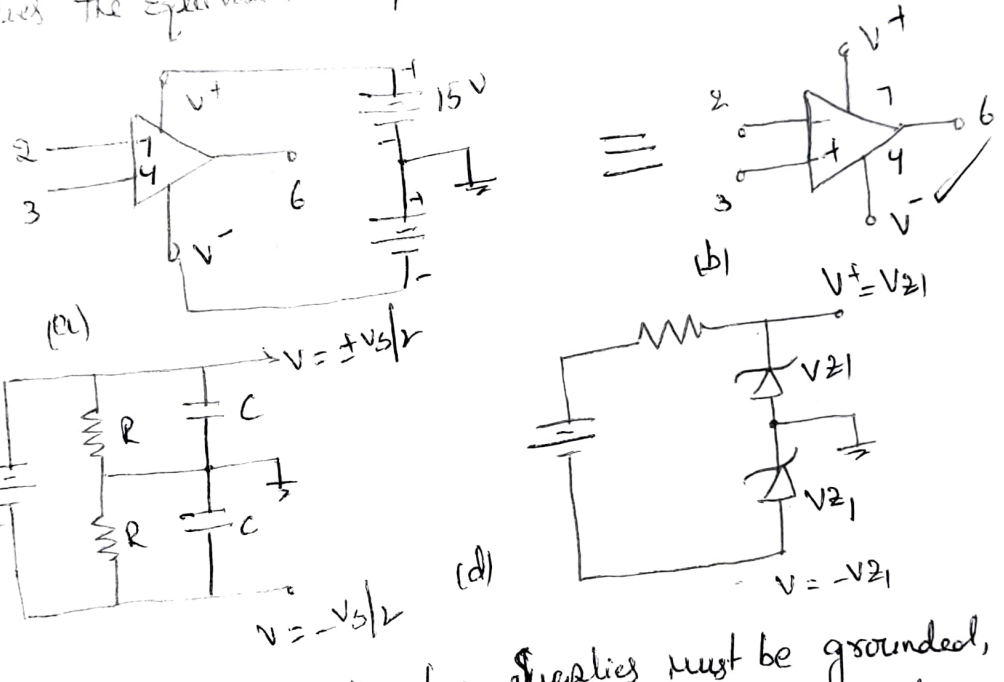
(c) 14pin dual in-line Package



(d) 10 pin flat pack

5. Power supply connections:-

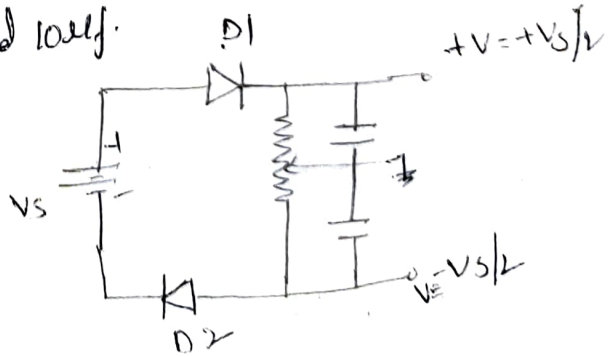
The V^+ and V^- power supply terminals are connected to two dc voltage sources. The V^+ pin is connected to the positive terminal of one source and the V^- pin is connected to the negative terminal of the other source as illustrated. Where the two sources are 15V batteries each. These are typical values, but in general, the power supply voltage may range from about ±5V to ±22V. The common terminal of the V^+ and V^- sources is connected to a ref point or ground. Some op-amp have a ground terminal but most do not. The ground is simply a convenient point on the circuit bread-board to which the op-amp is connected through the power supplies. The equivalent representation is shown fig.



The common point of the two supplies must be grounded, otherwise twice the supply voltage will get applied and it may damage the opamp. Instead of using two power supplies one can use a single power supply to obtain V^+ and V^- as shown in ckts resistor R should be > 10kΩ, so that it does not draw and more current from the supply V_S. The capacitors provide decoupling of the power supply range in value from 0.01 and 10μf.

In ckt (d) zener diodes are used to give symmetrical supply voltages

The value of the resistor Rs is chosen



such that, supplies sufficient current for the zener diodes to operate in the avalanche mode. In fig (e) Potentiometer is used to get equal values of V^+ and V^-. Diode D_1 and D_2 Protect the IC if the +ve and -ve leads of the supply voltage V_s are accidentally reversed. The diode can also be connected in shown in fig

The ideal operational Amplifier: - and Practicle specifications :-

The schematic symbol of an op-amp is shown in fig. It has two input terminals and one output terminal. other terminals have not been shown for simplicity. the − and + symbols at the input refer to inverting and non-inverting input terminals respectively. ie if $V_1 = 0$, output V_0 is 180° out of phase with input signal V_2. And, when $V_2 = 0$, output V_0 will be in phase with the input signal applied at V_1. This op-amp is said to be ideal if it has the following characteristics

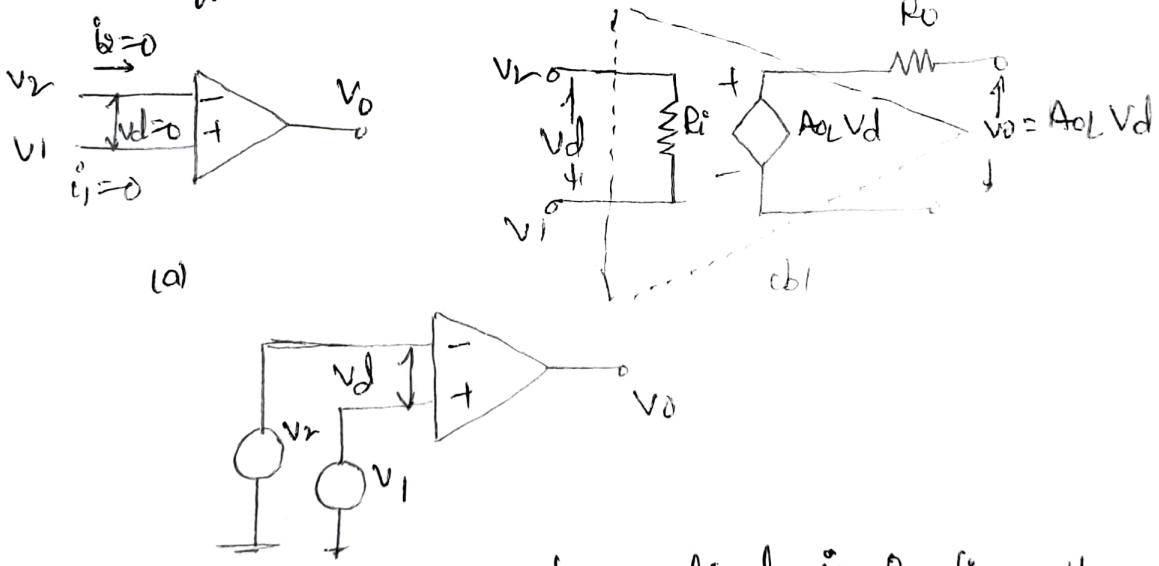
Open loop voltage gain = $A_{OL} = \infty$

Input impedence $R_i = \infty$

output impedence $R_o = 0$

Bandwidth $BW = \infty$

zero offset ie $V_0 = 0$ when $V_1 = V_2 = 0$



The above properties can never be realized in practice. However the use of such an 'ideal op-Amp' model simplifies the mathematics involved in op-Amp circuits. There are practical op-Amps that can be

...ble to approximate some of these characteristics.

A physical amp is not an ideal one. So the Equivalent ckt of an op-amp may be shown in fig. where $A_{OL} \neq \infty$, $R_i \neq \infty$; and $R_o \neq 0$. Note that $A_{OL} V_d$ is an Equivalent Thevenin voltage source and R_o is the Thevenin Equivalent resistance looking back into the output terminal of an op-amp. The Equivalent ckt is useful in analyzing the basic operating principles of Op-amp. For the Circuit is shown, the output voltage is

$$V_o = A_{OL} V_d$$
$$= A_{OL} (V_1 - V_2)$$

The Equations shows that the op-amp amplifies the difference between the two input voltages.

Open loop op-amp Configurations:-

In the case of amp the term (op-amp) open loop indicates that no connection (either direct (or) via another network, Exists between the o/p and i/p terminals. ie the o/p s/g is not feedback in any form as part of the i/p s/g and the loop that would have been formed with feedback is open. There are 3 Configurations

1. Differential amp
2. Inverting amp
3. Non Inverting amp

These Configuration are classed according to the no. of i/p used and the terminal to which the i/p is applied when a single i/p is used.

1. Differential Amp:-

$$V_o = A(V_{in1} - V_{in2})$$

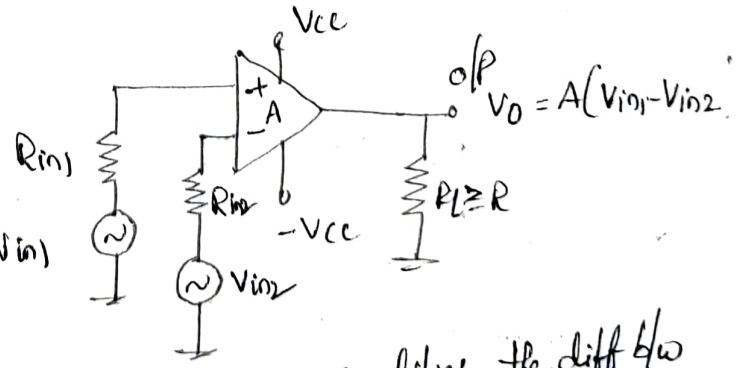


fig shows the open loop diff amp in when i/p signals V_{in1} & V_{in2} are applied to +ve and -ve i/p terminals. the opamp amplifies the diff b/w the two i/p s/gs, this configuration is called diff amp.

Feed back in Ideal Opamp:-

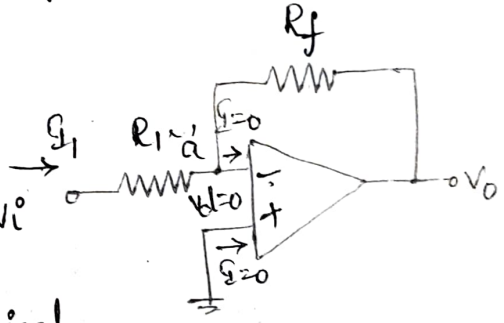
The utility of an opamp can be greatly increased by providing negative feedback. The output in this case is not driven into saturation and the circuit behaves in a linear manner.

Two important Negative feedback circuits used. In order to understand the operation of these circuits, we make too realistic simplifying assumption like 1) The current drawn by either of i/p terminals is negligible.

2) The differential input voltage V_d between Non-Inverting and Inverting i/p terminals is essentially zero.

2. The Inverting Amp:-

This is most widely used of all the op-amp circuits. The circuit is shown in fig. The output voltage V_o is fed back to the Inverting i/p terminal through the R_f-R_1 network where R_f is the feedback resistor. Input sig V_i is applied to the Inverting i/p terminal through R_1 and Non-inverting i/p terminal of opamp is grounded.



Analysis:- For simplicity, assume an ideal opamp, as $V_d = 0$, node 'a' is at ground potential and the current I_1 through R_1 is

$$I_1 = \frac{V_i}{R_1}$$

$$V_o = -I_1 R_f = -V_i \frac{R_f}{R_1}$$

Hence the gain of Inverting amp $A_{CL} = \frac{V_o}{V_i} = \frac{-R_f}{R_1}$

alternatively, the nodal equation at the node 'a' in fig is

$$\frac{V_a - V_i}{R_1} + \frac{V_a - V_o}{R_f} = 0$$

where V_a is the voltage at node 'a'. Since node 'a' is at virtual ground.

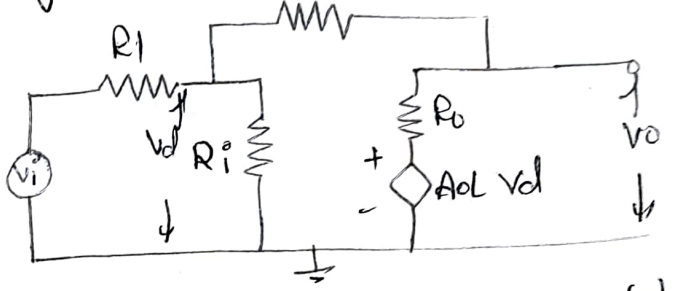
$V_a = 0$

$$\therefore A_{CL} = \frac{V_o}{V_i} = \frac{-R_f}{R_1}$$

the -ve sign indicates a phase shift of 180 b/w V_i and V_o. Also since inverting input terminal is at virtual ground, the effective i/p impedance is R_1. The value of R_1 should be kept fairly large to avoid loading effect.

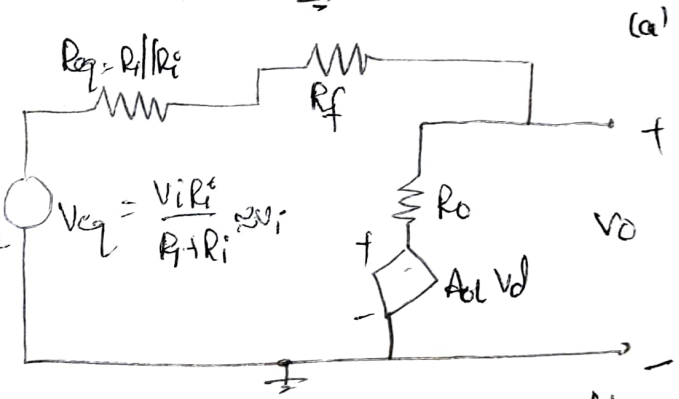
Practical Inverting Amplifier:-

In a practical op amp, the expression for the closed loop voltage gain should be calculated using the low frequency model. the Equivalent circuit of a practicle inverting amp is shown in fig.



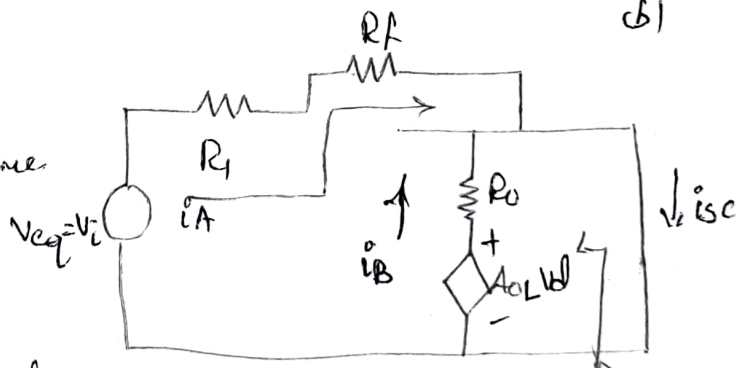
(a)

the can be simplified by replacing the signal source V_i and resistor R_i by Thevenin's Equivalent as shown in fig. which is analysed to calculate the exact expression for Closed loop gain, A_{CL} and i/p impedance Rif.



(b)

The input impedance Ri of an op-amp is usually much greater than R_1. So one may assume $V_{eq} \cong V_i$ and $R_{eq} \cong R_1$



(c)

From o/p loop $V_o = iR_o + A_{OL}V_d$ —①

for fig(b) $V_d + iR_f + V_o = 0$ —②

Putting V_d value in Eqn ①

$$V_o(1 + A_{OL}) = i(R_o - A_{OL}R_f) \quad \text{—③}$$

Also the KVL loop equation is

$$V_i = i(R_1 + R_f) + V_o \quad \text{---} (4)$$

Putting the value of i by (3) Eq in (4)

$$i = \frac{V_o (1 + A_{OL})}{R_o - A_{OL} R_f}$$

$$V_i = \frac{V_o(1 + A_{OL})}{R_o - A_{OL}R_f} (R_1 + R_f) + V_o$$

$$A_{CL} = \frac{V_o}{V_i} = \frac{R_o - A_{OL}R_f}{R_o + R_f + R_1(1 + A_{OL})} \quad \text{---} (5)$$

it can be seen from equation (5) that if $A_{OL} \gg 1$ and $A_{OL} R_1 \gg R_o + R_f$

and neglect $\boxed{A_{CL} \approx -\frac{R_f}{R_1}}$

Input Resistance R_{if}

From fig (b) $R_{if} = \frac{V_d}{i}$

writing loop Equation and solving for R_{if}

$$V_d + i(R_f + R_o) + A_{OL} V_d = 0.$$

$$V_d [1 + A_{OL}] + i(R_f + R_o)$$

$$\frac{V_d}{i} = -\frac{R_f + R_o}{1 + A_{OL}}$$

$$\boxed{R_{if} = \frac{R_f + R_o}{1 + A_{OL}}}$$

Output Resistance R_{of}:- output impedance R_{of} (without R_L) is calculated from the open circuit output voltage V_{oc} and short ckt ise Now the circuit from c is $i_A = \frac{V_i - 0}{R_1 + R_f}$.

$$i_B = \frac{A_{OL} V_d}{R_o}$$

$$V_d = -i_A R_f$$

$$i_B = -\frac{A_{OL} i_A R_f}{R_o}$$

Sol $i_{sc} = i_A + i_B$ we obtain $V_i \frac{(R_o \ominus A_{OL} R_f)}{R_o(R_1 + R_f)}$

$$R_{of} = \frac{V_{oc}}{i_{sc}}$$

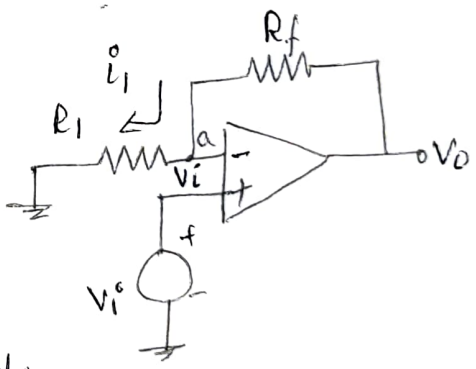
and $A_{cl} = \frac{V_{oc}}{V_i}$

$$\therefore R_{of} = \frac{A_{cL} V_i}{V_i \left[R_o - A_{OL} R_f / R_o(R_1 + R_f) \right]}$$

Putting A_{cL} $R_{of} = \frac{R_o(R_1 + R_f)}{R_o + R_f + R_1(1 + A_{OL})}$

It may be seen that numerator consists of a term $R_o // (R_1 + R_f)$ and is therefore smaller than R_o.

(3) The Non-Inverting Amplifier:-



If a signal (ac & dc) is applied to the Non-inverting input terminal and feedback is given as shown in fig. the ckt amplifies without inverting the input signal. Such a circuit is called Non-Inverting amplifier.

It may be noted as that is also a negative feedback system as o/p is being fed back to the inverting input terminal.

As the differential voltage V_d at the i/p terminal of op-amp is zero, the voltage at node 'a' in fig. 6 is V_i, same as the input voltage applied to Non-inverting input terminal. Now R_f and R_1 forms

a potential divider Hence

$$V_i = \frac{V_o}{R_1+R_f} R_1$$

as no current flows into the op-amp

$$\frac{V_o}{V_i} = \frac{R_1+R_f}{R_1} = 1 + \frac{R_f}{R_1}$$

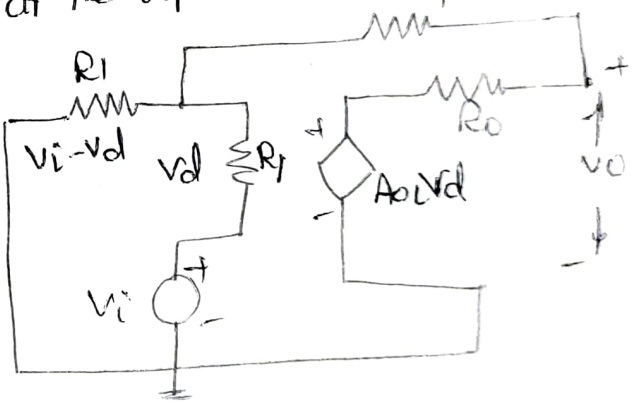
Thus, for non-inverting amplifier the voltage gain

$$A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

The gain can be adjusted to unity or more, by proper selection of resistors R_f and R_1 compared to the inverting amp. the i/p resistance of the non-inverting amp is extremely large ($=\infty$) the opamp draws negligible current from the signal source.

Practical Non-Inverting Amp:-

The analysis of non-inverting amp can be performed by using the equivalent circuit shown in fig. writing KCL at the input node



similar at output node, KCL gives

at the input node,

$$(V_i - V_d)Y_1 + V_d Y_i + (V_i - V_d - V_o)Y_f = 0$$

$$-(Y_1 + Y_i + Y_f)V_d + (Y_1 + Y_f)V_i = Y_f V_o$$

similarly at o/p node KCL gives

$$(V_i - V_d - V_c)Y_f + (A_{OL}V_d - V_o)Y_o = 0$$

$$-(Y_f - A_{OL}Y_o)V_d + Y_f V_i = (Y_f + Y_o)V_o$$

Now solving for V_o/V_i we get

$$A_{CL} = \frac{V_o}{V_i} = \frac{A_{OL}Y_o(Y_1+Y_f) + Y_f Y_i}{(A_{OL}+1)Y_o Y_f + (Y_1+Y_i)(Y_f+Y_o)}$$

if $A_{OL} \to \infty$, reduce to $A_{CL} \simeq \frac{A_{OL}Y_o(Y_f+Y_f)}{A_{OL}Y_o Y_f}$

$$A_{CL} = \frac{V_1 + V_f}{V_1} = 1 + \frac{V_f}{V_1}$$

$$\boxed{A_{CL} = 1 + \frac{R_f}{R_1}}$$

DC Characteristics of an Op-amp:-

An ideal op amp draws no current from the source and its response is also independent of the temperature. But real op-amp does not work this way. Current is taken from the source into the op-amp i/ps. Also the two inputs respond differently to current and voltage due to mismatch in transistor. A real op-amp also shifts its operation with temp. these Non-ideal dc characteristics that add error components to the dc o/p voltage. So that the DC characteristics are (1) Input Bias Current.

(2) Input offset Current

(3) Input offset Voltage

(4) Total offset voltage

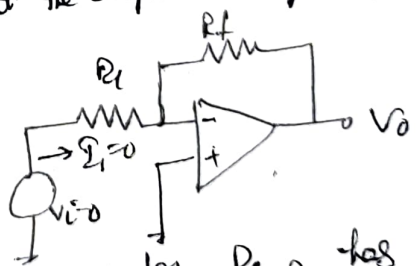
(5) Thermal drift.

(1) **Input Bias Current**:- I_B as the average value of the base currents entering into the terminals of an op-amp.

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

for an op-amp $I_B \cong 500nA$.

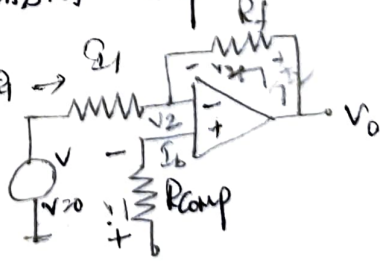
Consider the basic inverting amplifier if i/p $V_i = 0$, the output voltage V_o should be zero. Instead of we find. that the output voltage is offered by



$$V_o = (I_B^-) R_f \text{ if } R_f = 1M\Omega$$

$$V_o = 500nA \times 1M = 500mV$$

To compensate this by the compensation resistor R_{comp} has been added between the non-inverting terminal



$$-V + 0 - V_2 - V_o = 0$$

$$V_o = V_2 - V_1$$

In selecting proper value of

R_{comp} V_2 can be cancelled with V_1 & V_o will be zero

the value of R_{comp} is $V_1 = I_B^+ R_{comp}$

$$I_B^+ = \frac{V_1}{R_{comp}}$$

Input voltage at node 'a' is at voltage $(-V_1)$ because of the at non inverting input terminal is $(-V_1)$

$V_i = 0$

$$I_1 = \frac{V_1}{R_1}$$

for compensation V_o is 0 at $V_i = 0$ then $V_1 = V_2$

$$I_2 = \frac{V_1}{R_f}$$

KCL $\quad I_B^- = I_2 + I_1 = \frac{V_1}{R_1} + \frac{V_2}{R_f} \qquad V_1 \left[\frac{R_1 + R_f}{R_1 R_f} \right]$

$$I_B^- = I_B^+ = \frac{V_1}{R_{comp}}$$

$$R_{comp} = R_1 \| R_f$$

Input offset current :- Bias current will work with ideal; if both bias current are equal. if the input transistors can't be made identical, there will be a difference between the I_B^+ & I_B^-. so it is called input offset current $\quad |I_{os}| = I_B^+ - I_B^- \simeq 200nA$

$V_1 = R_{com} I_{B_1} \quad \left| V_1 = I_B^+ \cdot R_{comp} \right.$

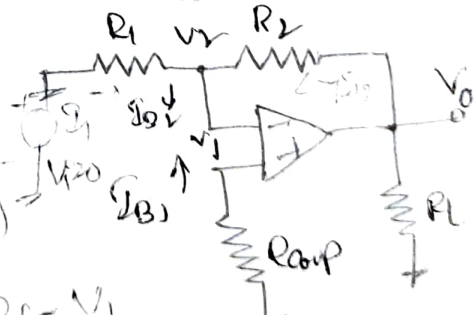
$V_2 = R_f I_{B_2} \quad \left| I_2 = (I_B^- - I_1) \right.$

$V_o = -R_f I_{B_2} \quad \left(I_B^- - I_B^+ \frac{R_{comp}}{R_1} \right)$

$V_o[I_{B_1} = V_1 \left[1 + \frac{R_f}{R_1} \right]$

$V_o[I_{B_1} = R_{com} I_{B_1} \left[1 + \frac{R_f}{R_1} \right]$

$= \frac{R_1 R_f}{R_1 + R_f} I_{B_1} \frac{R_1 + R_f}{R_1} = R_f I_{B_1}$



$$V_0 I_{B1} = R_f I_{B1}$$

$$V_0 I_{B1} + V_0 I_{B2} = R_f I_{B1} - R_f I_{B2}$$

$$= R_f [I_{B1} - I_{B2}]$$

$$\boxed{V_0 I_{io} = R_f I_{io}}$$

$V_0 = R_f [I_{B1} - I_{B2}]$

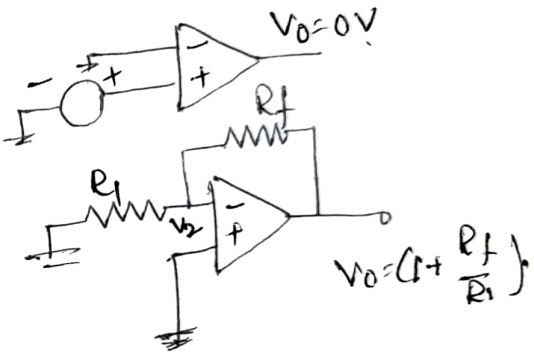
$V_0 = 200mV$

R_{f2} small

$R_1 \uparrow \rightarrow V_0 \downarrow$

Input offset Voltage:- It is an amount of i/p voltage that would be applied between two input signal in order to force the o/p V is 0. Let us denote the o/p offset voltage due to i/p offset voltage V_{ios} V_{oo}. This is caused by mismatching between two input terminals. Even though all components are integrated on the same chip, it is not possible to have two transistors in the i/p diffrence amp stage with Exactly the same characteristic ie β's are not same

If V_i is set to 0, the Circuits of inverting and Non-Inverting will be some. So that the voltage V_2 at the -ve terminal is



$$V_2 = \frac{R_f}{R_1 + R_f} V_0 \quad ; \quad V_0 = \frac{R_1 + R_f}{R_1} V_2$$

$$V_0 = \left[1 + \frac{R_f}{R_1}\right] V_2.$$

$$V_{io} = [V_i - V_2] = V_i - 0$$

$$V_{io,s} = |-V_2|$$

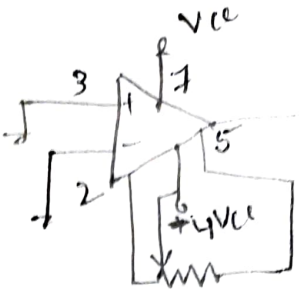
$$V_{ios} = V_2$$

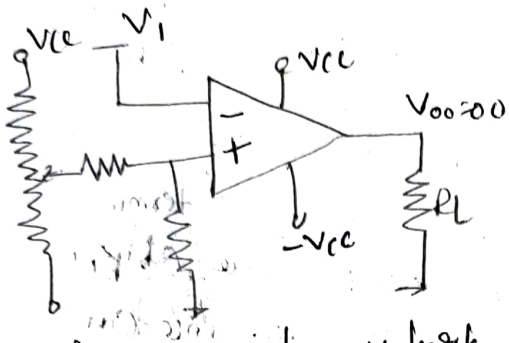
So that $V_0 = \left[1 + \frac{R_f}{R_1}\right] V_{ios}$ for closed loop config.

To reduce V_{oo} to zero we need a ckt at positive i/p terminals of the Op-amp that will give us the flexibility of obtaining

Vio of proper amp and polarity. Such a circuit is called Compensating Network

Off set Voltage Compensating Network.





the Compensating Network Consists of Potentiometer Ra & resistor Rb & Rc of we are planning to make Inverting amplifier, The Compensation Network should be Connected to the Non-Inverting terminal and Pot Ra, Rb have +Vcc & -Vcc, the voltage across Rc is voltage at inverting terminal V_2. By adjusting Ra, Pot, V_2 Can be made to Equal to V_1. ie Vio is zero which forces Voo is also o

Total offset Voltage:- we know that in the Circuit like Inverting feedback amplifier, the output offset voltage Voo Caused by Vio Could be either +Ve or -Ve w.r.to ground. Similarly the output offset voltage Caused by I_B Could be either +Ve (or) -Ve. So that the total(diff) offset voltage is

$$V_{OOT} = V_{OO} + V_O I_B$$

$$= \left(1 + \frac{R_f}{R_1}\right) V_{io} + (R_F) I_B$$

$$= \left(1 + \frac{R_f}{R_1}\right) V_{io} + R_F I_{io}$$

Thermal drift:- The parameters Vio, I_B, & I_{io} are Constant for a given Op-Amp However in practice the values of Vio, I_B, I_{io} vary with change in temp, power Supply, time.

The average rate of change of i/p offset Voltage per unit change in temperature is called Thermal drift by $\frac{\Delta V_{io}}{\Delta T}$ / 4V/°C → 15 °μV/°

$\frac{\Delta I_{IO}}{\Delta T}$ pA/°C ; $\frac{\Delta I_{IB}}{\Delta T}$ / pA/°C → 200 pA/°C

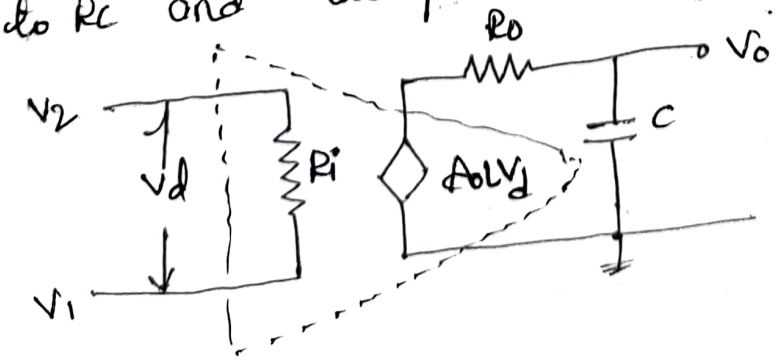
PSRR:- The change in op-Amp input offset voltage caused by variation in supply voltage is generally specified by a variety of terms power supply rejection ratio; input offset sensitivity, supply voltage Rejection ratio.

Common Mode Rejection Ratio:- It is a ratio of common mode Gain to Differential Mode gain. CMRR = $\frac{A_{CM}}{A_{DM}}$

Ac characteristics:- the Ac characteristics of op-Amp is 1) frequency Respons
2) Slew rate.

(1) Frequency Response:- Ideally, an op-Amp should have an infinite Bandwidth This means that, if its open-loop gain is 90db. with dc signal its gain should remain the same 90db through audio and on to high radio freq's. the practical op-amp gain, however decrease at higher frequencies.

The reason for the Gain of the op-Amp to roll-off a certain frequency is, there must be a capacitive component in the equivalent circuit of op-Amp. this capacitance is due to the physical characteristics of device used in the internal construction of an op-Amp. for an op-Amp with only one break frequency, all the capacitive effects can be represented by a single capacitor c as shown in fig. Consider that the low freq model of op-amp with a capacitor C at the o/p. there is one pole due to Rc and -20db/decade roll-off comes into effect.



The open loop voltage Gain of an op-Amp with only one Corner freq is obtained from the fig.

$$V_o = \frac{-jXC}{R_o - jXC} A_{OL} V_d.$$

$$A = \frac{V_o}{V_d} = \frac{A_{OL}}{1 + j2\pi f R_o C}$$

$$A = \frac{A_{OL}}{1 + j(f/f_1)} \quad \because f_1 = \frac{1}{2\pi R_o C}$$

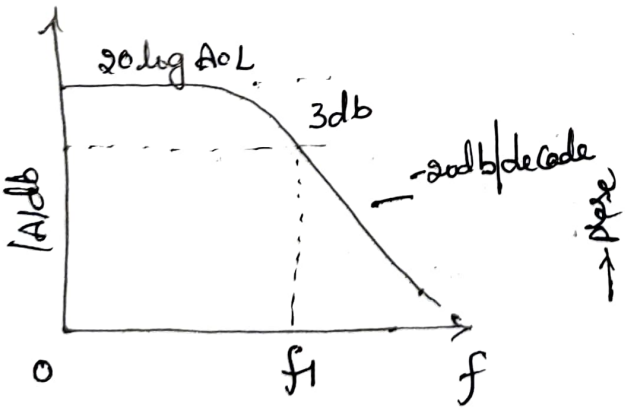
The magnitude and phase of the eq is

$$|A| = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}} \; ; \; \phi = -\tan^{-1}(f/f_1)$$

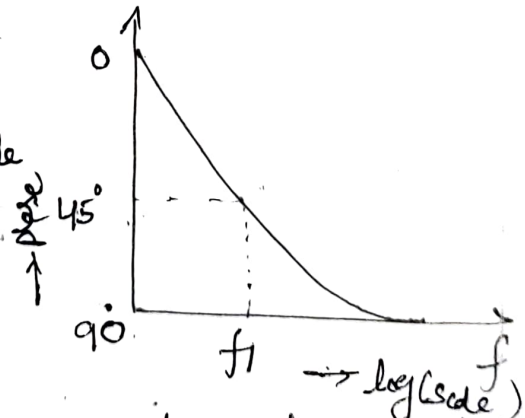
The magnitude and phase characteristics from the equations it can be seen that (i) For freq $f \ll f_1$, the magnitude of the Gain is $20 \log A_{OL}$ in db.

(ii) For $f \simeq f_1$, the Gain is 3db down from the dc value of A_{OL} Now the freq called as corner frequency.

(iii) For $f >> f_1$ the Gain rolloff at the rate of -20db/decade.



Magnitude characteristics



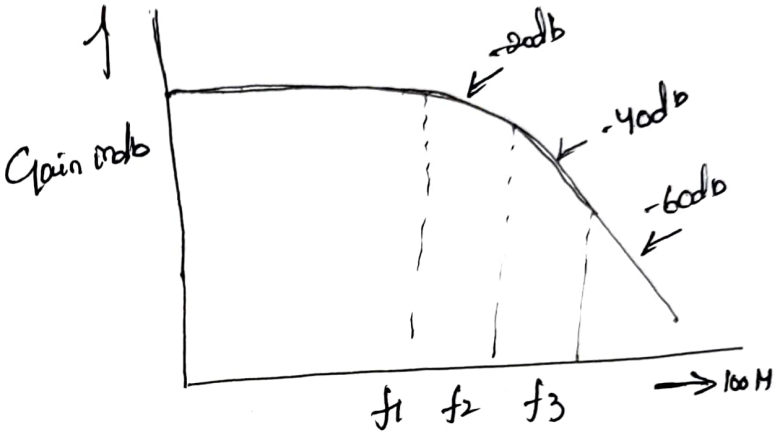
phase characteristics.

And further from the phase characteristics that the phase angle is zero at frequency $f = 0$, At corner freq f_1 the phase is $-45°$

and at finite frequency the phase angle is -90°.

A practical op-Amp, however no of stages produces a capacitive component. Thus due to a number of Rc pole pairs, there will be a no of different break frequencies. Then the transfer function of an op-Amp with 3 break frequencies can be assumed as

$$A = \frac{A_{OL}}{(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)} \quad \because 0 < f_1 < f_2 < f_3$$



2)

→ The Rise time of an amp is defined as the time the o/p take to change from 10 to 90 of the final value for a step i/p & is given by 0.35/BW.

→ for ideal response time should be zero and BW should be infinite.

→ Rise time is usually specified for small signals, usually when the peak o/p voltage is less than < 1V.

→ for large signals op-Amp's speed is limited by slew rate.

→ Manufacturers specify slew rate that gives the circuit designer a good idea of how quickly a given op-amp responds to changes of i/p voltage.

→ Usually op-Amps with wide bandwidth will have higher slew rate.

→ the slew rate is defined as the max rate of change of output voltage caused by a step i/p voltage and is usually specified in V/μs.

→ For example, a 1V/μs slew rate means that the o/p raises or falls by 1V in one μs.

→ An ideal slew rate is infinite which means o/p of op-Amps change instantaneously in response to i/p step voltage.

→ But as per the data sheet the range of slew rate is 0.1V/μs to 1000 V/μs

→ the slewrate improves with higher closed loop and dc supply.

→ It can also be a function of temp and Generally decrease with an increase in temp.

Derivation

→ There is usually a Capacitor within (or) outside an op-Amp to prevent oscillation. It is its prevents the o/p voltage from responding immediately to a fast changing i/p.

The rate at which the voltage across the Capacitor Vc increase is given by

$$\frac{dVc}{dt} = \frac{I}{C}$$

Here I is maximum current given by op-Amp to the Capacitor C. This means that obtaing faster slew rate i op-Amp have either small current (or) Higher current Compensating Capacitor

$$SR = \frac{dVo}{dt}\Big|_{max} = \frac{I_{max}}{C} = \frac{15\mu A}{30pf} = 0.5V/\mu s.$$

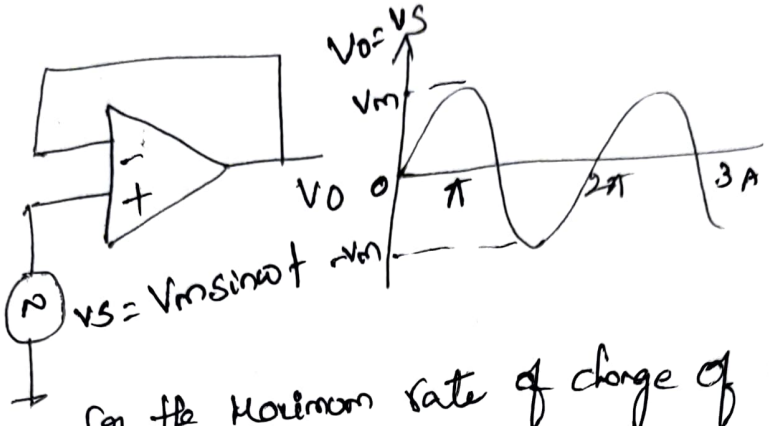
Slew rate limits the response speed of all large signals waveshapes. for a sine wave i/p the effect of slewrate limiting can be calculated as flows.

Consider a voltage follower shown in fig, the i/p is large amp, High freq sine wave if $V_s = V_m \sin \omega t$

then $V_o = V_m \sin\omega t$

The rate of change of the o/p is given by

$$\frac{dv_o}{dt} = V_m \omega \cos\omega t$$



for the maximum rate of change of o/p occurs when $\cos\omega t = 1$

i.e $$SR = \left.\frac{dv_o}{dt}\right|_{max} = \omega V_m$$

$\therefore$ slew rate $= 2\pi f V_m$ V/s.

$$\boxed{SR = \frac{2\pi f V_m}{10^6} \text{ V/}\mu\text{s}}$$

f = i/p freq
V_m = peak o/p amp

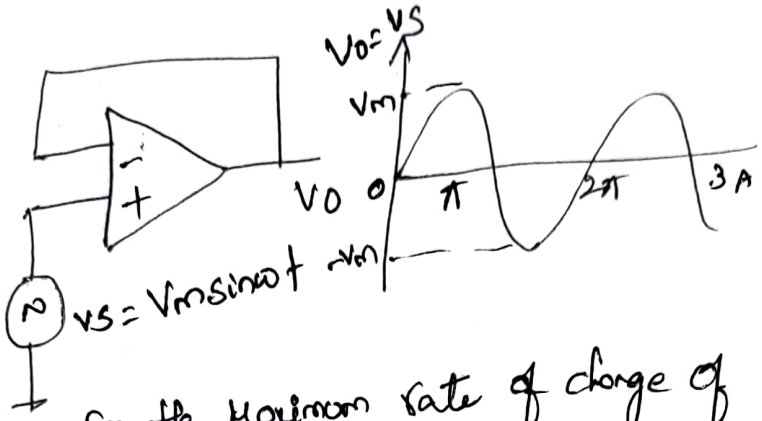
if this value of SR is < than SR of the op Amp, then o/p will be undistorted. If frequency (or) amplitude of i/p sig is increased by (exceed) slew rate, o/p is distorted.

Thus the max i/p frequency is $f_{max} = \frac{\text{Slew Rate}}{6.28 \times V_m} \times 10^6$.

then $V_o = V_m \sin\omega t$

The rate of change of the o/p is given by

$$\frac{dv_o}{dt} = V_m \omega \cos\omega t$$



for the maximum rate of change of o/p occurs when $\cos\omega t = 1$

i.e $$SR = \left.\frac{dv_o}{dt}\right|_{max} = \omega V_m$$

$\therefore$ Slewrate $= 2\pi f V_m$ V/s.

$$SR = \frac{2\pi f V_m}{10^6} \text{ V/}\mu\text{s}$$

f = i/p freq
V_m = peak o/p amp

if this value of SR is < than SR of the op Amp, then o/p will be undistorted. If frequency (or) amplitude of i/p sig is increased by (exceed) slewrate, o/p is distorted.

Thus the max i/p frequency is $f_{max} = \frac{\text{SlewRate}}{6.28 \times V_m} \times 10^6$.

Frequency Compensation Techniques:

There are two types of Compensation techniques

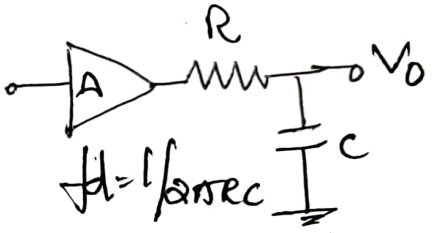
(1) External Compensation (2) Internal Compensation.

External Compensation:- Some types of op-Amp are made to be used with Externaly Connected Compensation Components specially if they are to be used for relatively low closed loop Gain. The Compensating networks alters the open-loop Gain, so that the roll-off is -20db/dec over a wide range frequency.

The Common Methods are (1) Dominant-pole Compensation.
(2) pole-zero compensation.

Dominant pole Compensation:-

Suppose 'A' is the uncompensated transfer-function of op-Amp in open-loop Condition. Introduce a Dominant pole by adding RC Network in series with op-Amp. (or) by Connecting 'C' from a suitable high resistance point to ground., The Compensation transfer function $A' = \frac{V_o}{V_i}$



$$= A \cdot \frac{-j/\omega C}{R - j/\omega C} = \frac{A}{1 + jf/f_d} \quad \because f_d = \frac{1}{2\pi RC}$$

$$A' = \frac{A_{OL}}{(1+jf/f_d)(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)}$$

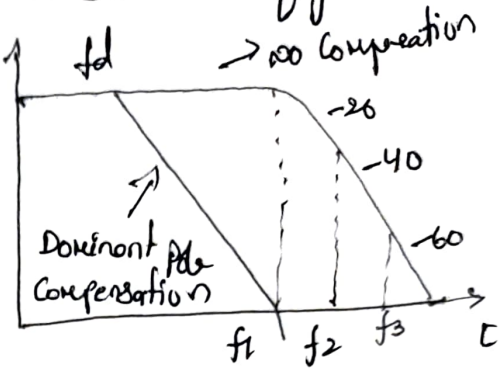
where $f_d < f_1 < f_2 < f_3$.

The Capacitance C is chosen so that the modified loop Gain drops to 0db with a slope of -20db/decade at the freq where the poles of uncompensated transfer fun A passes through 0db at the pole f_1

of the uncompensated A.

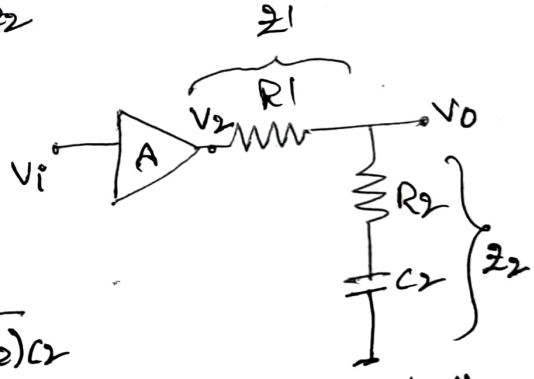
→ the freq can be found graphically by having A' pass through 0 db at freq f_0 with a slope of -20 fdb as shown in fig.

→ one dis-advantage of this compensating technique is it reduces the open-loop Bandwidth drastically. But the Noise immunity of the system is proved since the Noise frequency components outside the B.W is eliminated.



Pole-Zero Compensation:- Here the uncompensation transfer function A is altered by adding both pole and a zero as shown in fig. the zero should be at higher frequency than pole. The transfer function of Compensating Network alone is $\frac{V_0}{V_2} = \frac{Z_2}{Z_1+Z_2}$

$$= \frac{R_2}{R_1+R_2} \frac{1+jf/f_1}{1+jf/f_0}$$



Where $Z_1 = R_1$; $Z_2 = R_2 + \frac{1}{j\omega C_2}$. $f_1 = \frac{1}{2\pi R_2 C_2}$

$$f_0 = \frac{1}{2\pi(R_1+R_2)C_2}$$

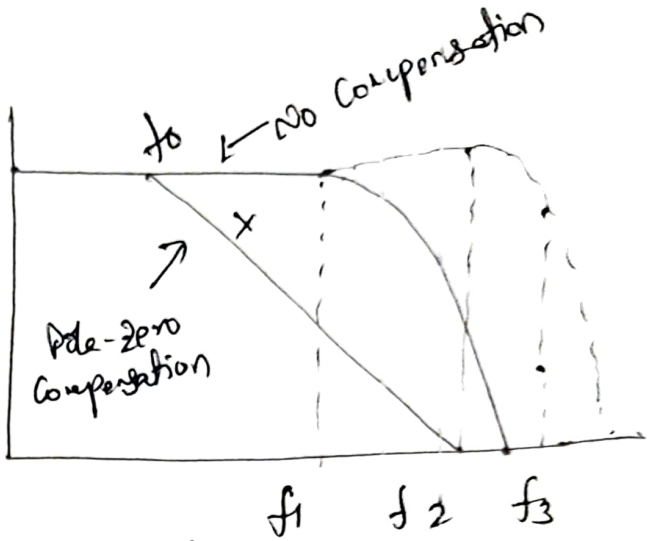
The Compensating Network is designed to produce a zero at the first freq (corner) of the uncompensated transfer function A. This zero will Cancle the effect of the pole at f_1.

$$A' = \frac{V_0}{V_i} = \frac{V_0}{V_2} \cdot \frac{V_2}{V_i}$$

$$= A \cdot \frac{R_2}{R_1+R_2} \frac{1+jf/f_1}{1+jf/f_0} = \frac{A_{OL}}{(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)} \times \frac{R_2}{R_1+R_2} \frac{1+jf/f_1}{1+jf/f_0}$$

$$= \frac{A_0 L}{(1+j f/f_0)(1+j f/f_2)(1+j f/f_3)} \quad 0 < f_0 < f_1 < f_2 < f_3.$$

if $R_2 \ll R_1$; $\frac{R_2}{R_1+R_2} = 1$.

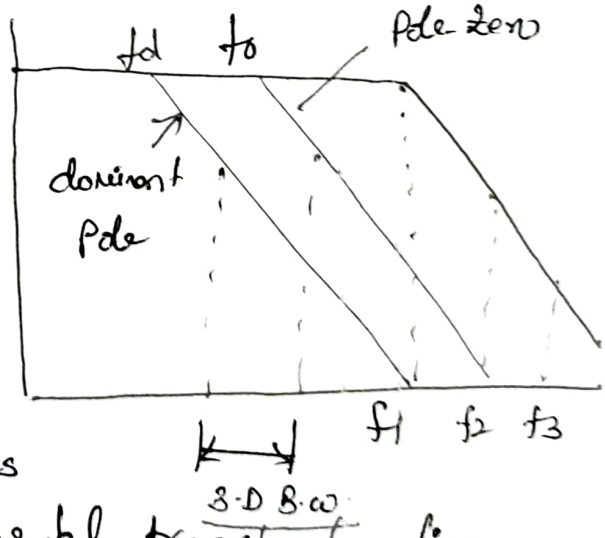


→ consider again the freq response for the uncompensated op-Amp 3 poles are at frequ's $f_1 f_2 f_3$. Now select $R_2 C_2$ so that the zero of the compensating N.W Equal to the pole at freq f_1. If there had been no pole added by the Compensating Network, the response would have to that of the dotted curve.

→ However, because of the predominance of the pole of the Compensating network at f_0 the rate of Closure will be -20db/decade.

→ the pole at f_0 should be selected so that -20db/decade fall should meet the 0db line at f_2 which is 2nd pole. A.

→ A Comparision of dominant pole and pole zero Compensation Technique is shown in fig.



→ the dominant pole is selected so that the compensation transfer function goes through 0db at the first pole f_1 the uncompensated system.

→ In a pole-zero Compensation, the zero is chosen at f_1 and pole is selected so that the modified transfer function goes through 0-db at 2nd pole f_2 of uncompensated transfer function.

→ the improvement of Bandwidth is clearly shown in fig, and it is given by $(f_2 - f_1)$

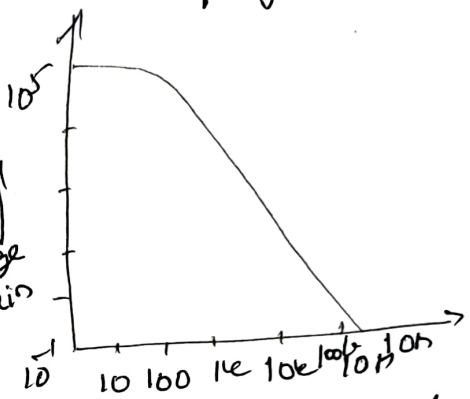
Internal Compensated Op-Amp:-

→ Some times the relatively broad bandwidth of the uncompensated op-Amp is not needed.

→ for example, in the instrumentation ckt, the op-Amp require to amplify relatively slow changing signals and therefore it doesnot require good high freq response.

→ In this and similar applications, internally compensated op-Amp can be used. They are sometimes called compensated op-Amp.

→ for op-Amp 741 is compensated and has an open loop gain Vs freq response.



→ the op-Amp IC741 contains a capacitance C_1 of 30pF, that internally shunts off sig current and thus reduces the available o/p sig at high freq's.

→ this internal capacitance, which is an internal compensating component, causes the open-loop gain to roll-off at -20db/decade rate and thus assures for a stable ckt.

→ the 741 op-Amp has a 1MHz gain-bandwidth product.

→ this means that the product of co-ordinates, gain and freq of any point on the open-loop gain Vs freq curve is about 1MHz.

→ If 741 op-Amp is wired for a closed loop gain of 10^4 ⇒ 80db its BW is 100Hz. as can be seen by projecting to the right from 10^4 in the curve as shown in fig.