Wave-form Generators Using Op-amps

Unit - IV

The op-amps are widely used in circuits for generating various wave-forms. Most of the analog & digital Equipment require one (or) more periodic wave-forms for timing, Control & other functions.

→ The Commonly used wave-form generators used in the design of op-amps are, sinusoidal, Square & Triangular wave-forms. This application of op-amps have made the design of oscillators

→ Now, in this chapter we will see, the use of op-amp as oscillators, which are capable of generating a variety of op waveforms.

→ Basically, the function of an oscillator is to generate alternating current (or) voltage wave-forms. More precisely an oscillator is a ckt. that generates a repetitive wave-form of fixed amplitude & freq. without any External i/p signal.

→ The terms "Oscillator" & "function generator" (or) "wave-form generator" represent the ckts employed for generating such wave-forms. Oscillators are used in Radio, Television, Computers & Communications.

Basic principle of Oscillator:-

Oscillator is a type of feed back amp, in which, part of the o/p is fed back to the i/p via a feedback ckt. as shown in fig:

→ If the signal fed back is of proper magnitude & phase the ckt produces alternating currents (or) voltages.

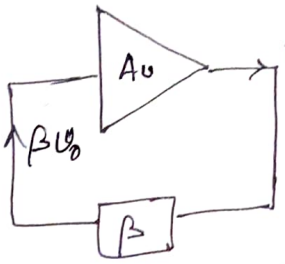


fig: Basic block diagram of oscillator.

→ Two requirements for Oscillations

* The magnitude of the loop gain i.e $|A_v\beta|$ should be > '1' for small signal levels & $A_v\beta = 1$ for desired o/p voltage amplitude

* The total phase shift produced around the loop must be 0° (or) 360°.

→ If the Amp: produces a phase of 180°, the feedback ckt, must provide an additional phase shift of 180°, so that the total phase shift is 360°.

⇒ The type of waveform generated by an oscillator depends on the components in the ckt, & hence may be sinusoidal, square, (or) triangular. & the "freq: of oscillation" is determined by the components in feedback ckt.

Multivibrators :—

Multi → Many ; Vibrator → Oscillator

A ckt. which can oscillate at a no: of freq:s, is called a "multivibrator". These are a group of "regenerative ckts", that are used extensively in timing applications. Basically, there are three types:

→ Astable
→ Bistable
→ Monostable

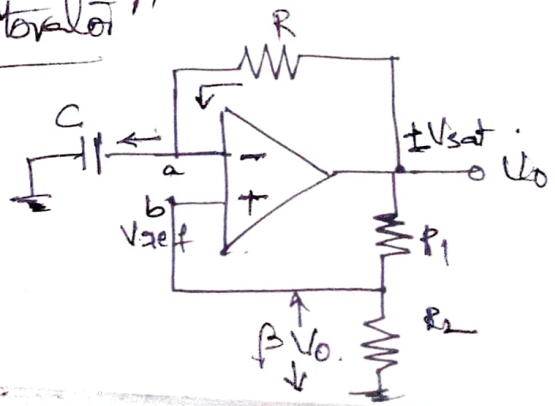
→ Each of these multivibrators has two states:

* Stable state :- is the state in which the device can stay permanently.

** Quasi stable state :- means temporary stable state

Astable multivibrator :- It is also known as "free running" multivibrator. The ckt has "two "Quasi stable" states". i.e no stable states. Thus, there is oscillations b/w these two states. & no external signal are required to produce the change in state.

→ Astable ckts are used to generate square waves, for Ex: clock generators in digital systems. Now let us see op-amp configured as "astable (or) free running symmetrical vibrator"



→ In free running mode, the two states are quasi-

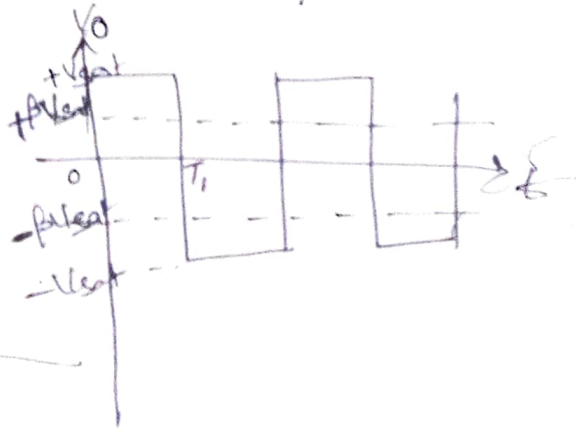
i.e the ckt switches repetitively b/w these two states. In one state, the amp: goes into "+Vsat" & while in the other state it goes to "−Vsat". Thus the amp: o/p is a "Square wave".

→ The period of the square wave is determined by the "time constant RC" & the feed back ratio established by the potential divider "$R_1 - R_2$". i.e $\beta = (R_2/R_1+R_2)$

→ Now let us see the operation of the ckt, here, we are not applying any i/p, but we are getting the o/p. But we are giving, the supply voltages for biasing, due to which, i/p bias-currents will flow & gives o/p voltage, which is fedback to the +ve i/p of op-amp.

→ Thus, the voltage at the i/p is nothing but the voltage across 'R_2' i.e βV_0. i.e $V_{out} = V_0$. & may take values as $+\beta V_{sat}$ (or) $-\beta V_{sat}$ as shown below.

→ The o/p is also fed back to the −ve i/p by means of low pass RC combination. whenever, the i/p at the −ve terminal just exceeds "Vout", switching takes place & gives the square wave o/p.



as $+V_{sat}$ & $-V_{sat}$

→ Now, Let us see, the voltage across the capacitor when the o/p is at $+V_{sat}$ & $V_{out} = +\beta V_{sat}$, the voltage across -ve i/p is also at same potential & the capacitor charges through the resistor 'R' until it has just exceeded $+\beta V_{sat}$ i.e "V_{ref}"

* When the voltage at -ve i/p becomes just greater than "V_{ref}", the o/p is driven into $-V_{sat}$ i.e, the Capacitor begins to discharge through 'R', towards $-\beta V_{sat}$. i.e When the o/p is "$-V_{sat}$" the capacitor discharges until "$-\beta V_{sat}$", & again o/p switches to $+V_{sat}$. & the cycle repeats itself as shown in fig.

→ Therefore, the astable multivibrator produces "square" & "sawtooth" waves.
↳ as o/p
↳ as 'V_c'.

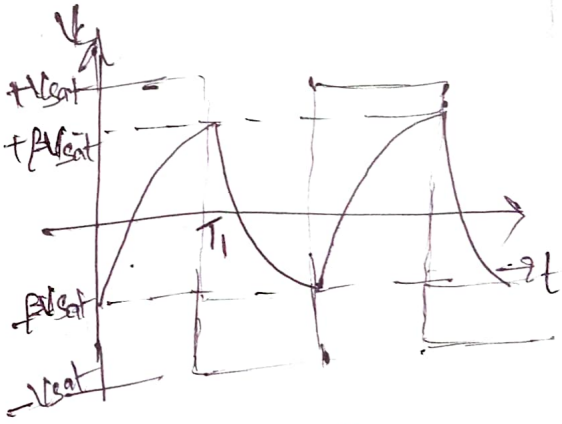


fig: Waveform across the capacitor.

→ Now, we have to find out the freq: of Oscillation, which is from the voltage across 'Vc'

* The freq: is determined by the time, it takes the Capacitor to change from $+\beta V_{sat}$ to $-\beta V_{sat}$ (or) Vice Versa

So, the voltage across the capacitor as a function of time is given by,

$$V_c(t) = V_f + (V_i - V_f)\, e^{-t/RC}$$

where, $V_f \rightarrow$ is the final value i.e, $+V_{sat}$.

$V_i \rightarrow$ is the initial value i.e, $-\beta V_{sat}$

$$\therefore V_c(t) = V_{sat} + (\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

$$= V_{sat} - V_{sat}(1+\beta)\, e^{-t/RC} \quad \rightarrow (1)$$

→ At $t = T_1$, the voltage across the capacitor reaches $+\beta V_{sat}$ & Switching takes places,

$$\therefore V_c(T_1) = \beta V_{sat}$$

$$= V_{sat} - V_{sat}(1+\beta)\, e^{-T_1/RC}$$

$$V_{sat}(1+\beta)\, e^{-T_1/RC} = V_{sat} - V_c(T_1)$$

$$e^{-T_1/RC} = \frac{V_{sat} - V_c(T_1)}{V_{sat}(1+\beta)}$$

$$V_{sat} - (\beta V_{sat}) \quad V_{sat}(1+\beta)$$

Apply log on both sides

$$e^{-T_1/RC} = \frac{V_{sat}(1+\beta)}{V_{sat}(1+\beta)}$$

$$\text{Eq} \quad \boxed{T_1 = RC \ln \frac{1+\beta}{1-\beta}}$$

$$\therefore \text{Total Time period } \& \text{ 'T'} = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta}$$

→ If $R_1 = R_2$, then $\beta = 0.5$ &

$$T = 2RC \ln(3)$$

For $R_1 = 1.16 R_2 \Rightarrow T = 2RC$

$$\therefore f_0 = \frac{1}{2RC}$$

→ i.e to depends only on external components.

The O/P swings from $+V_{sat}$ to $-V_{sat}$ So, peak to peak O/P $\boxed{V_0 = 2V_{sat}}$

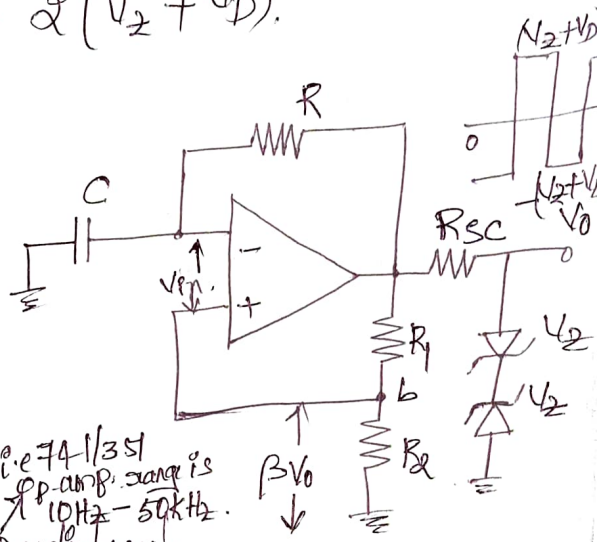
→ The peak-to-peak amplitude can be varied by varying the power supply voltages. However, a better tech: is used i.e by the use of "back to back zener diodes" as shown in below fig:

The o/p voltage is regulated to $\pm(V_z + V_D)$ by the zener diodes

$\therefore V_{o(pp)} = 2(V_z + V_D)$.

→ In this, the resistor "R_{sc}" limits the current drawn from the op-amp to,

$$I_{sc} = \frac{V_{sat} - V_z}{R_{sc}}$$



i.e 741/351 op-amp range is 10Hz – 50kHz.

fig: Use of back to back zener diodes

→ This ckt is applicable to Audio freq:s. At higher freq:s, other than this range is required. However, slew rate of the op-amp limits the slope of the o/p square wave., then the ckt should use zener diodes
↳ Three cct limits total o/p swing. & also prevent amp: from going into saturation

→ If an assymmetric square wave is desired, then the zener diodes with diff: breakdown voltages "V_{z1} & V_{z2}" may be used. Then the o/p is either "V_{o1}" (or) "V_{o2}", where,

$+V_{sat}$: $V_{o1} = V_{z1} + V_D$ where, V_D → forward diode volt: Drop = 0.7V

$-V_{sat}$: $V_{o2} = V_{z2} + V_D$.

+ve duration, $T_1 = RC \ln\left(\frac{1+\beta V_{o2}/V_{o1}}{1-\beta}\right)$

-ve duration, $T_2 = RC \ln\left(\frac{1+\beta V_{o1}/V_{o2}}{1-\beta}\right)$.

→ An alternative method, to get assymmetric square wave o/p is to add a "d.c" voltage source "V" in series with "R_2". as shown in below fig.

→ Now, the capacitor 'c', swings b/w the voltage levels $(\beta V_{sat} + V)$ & $(-\beta V_{sat} + V)$.

→ If the voltage source 'V', is made variable, voltage to freq. conversion can be achieved, though the variation will not be ~~zero~~ linear.

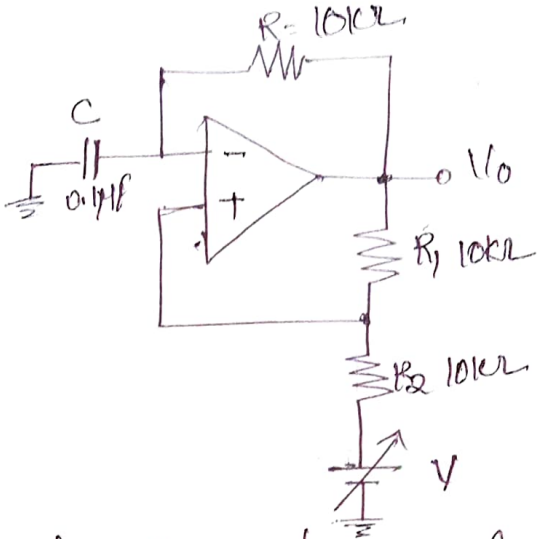
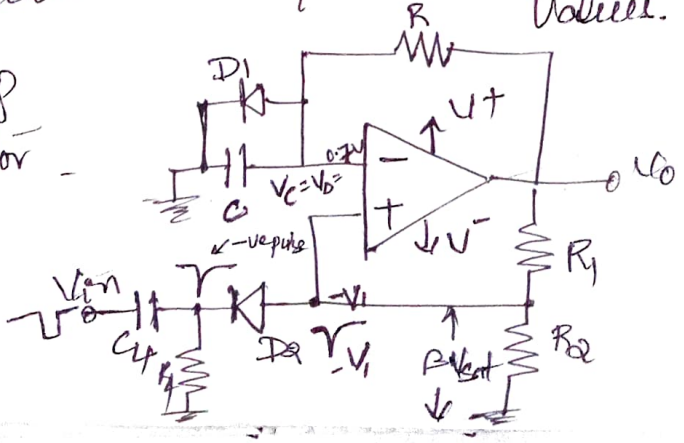


fig: Assymmetric square wave generator

Monostable multivibrator :—

Monostable multivibrator has "one stable" state & the other is "quasi stable" state. It can be made to switch to other state by ~~the~~ applying a "triggering pulse", but, it then reverts to its stable state after a time interval determined by the ckt component values.

→ Now, Let us see, the op-amp as, monostable multivibrator as shown in fig:



→ At the inverting i/p, the Connection of diode 'D' in parallel with the timing Capacitor 'C', is used to prevent the inverting i/p of the op-amp from going positive, thus, it results monostable multivibrator.

→ The diode 'D1', clamps the Capacitor voltage to 0.7V, when the o/p is at +Vsat. At the non-inverting i/p, the Capacitor 'C1' & Resistor 'R1', forms the differentiator which is followed by Diode 'D2', through which a -ve going pulse signal of magnitude 'Vi' is applied @ the -ve i/p terminal (i.e triggering pulse the diode produces, -ve pulse)

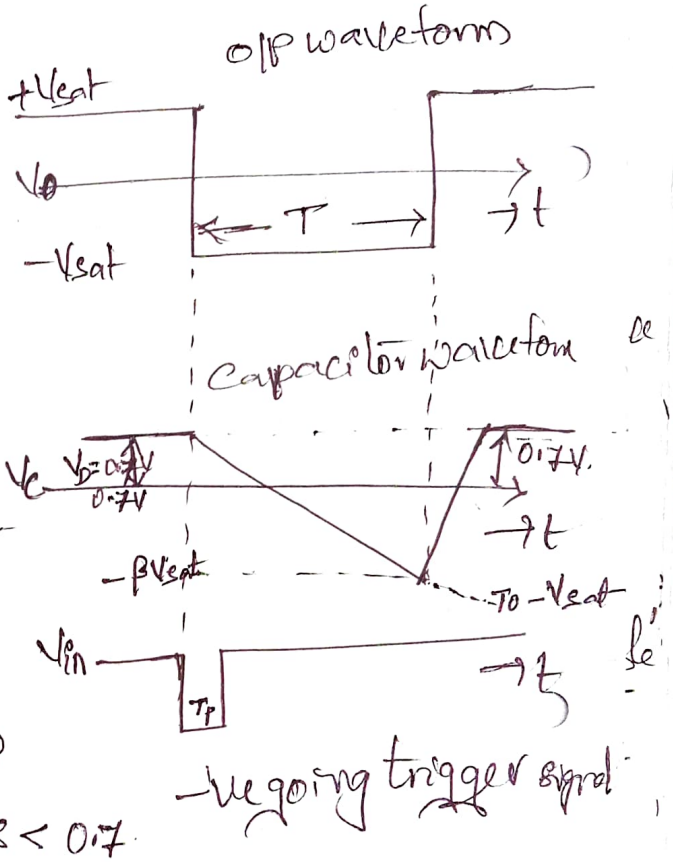
→ Here, 'R1' is assumed to be greater than 'R2', so that, its loading effect may be neglected. The diode 'D2', avoids any +ve noise spike present in the trigger pulse.

→ Now Let us see the analysis for this, Initially, assume that, in the stable state, the o/p, Vo is at "+Vsat". The voltage at +ve i/p, through potential divider R1 R2 is "+βVsat". So the diode 'D1' conducts & the voltage across it, Capacitor 'Vc' gets clamped to +0.7V. In order for switching i.e to go to -Vsat, we will apply

→ Now, if a -ve, trigger pulse of magnitude 'Vi' is applied to the +ve i/p, so that, the effective signal, at this terminal is less than 0.7V i.e $\boxed{\beta V_{sat} + (-V_i) < 0.7\,V.}$, then the o/p of the op-amp will switch from +Vsat to -Vsat.

→ Now, the diode 'D1' is reverse biased & the Capacitor starts discharging exponentially to "-Vsat" through the resistor 'R'. (since 'Vsat')

→ When the O/P is $-V_{sat}$, the voltage at +ve I/P is $-\beta V_{sat}$. (switching takes place) When the capacitor voltage 'V_c', becomes just slightly more -ve than "$-\beta V_{sat}$", the O/P of the op-amp switches back to "$+V_{sat}$" through 'R' until 'V_c' is 0.7V. as capacitor 'C' gets clamped to the voltage as shown in the wave forms.



-ve going trigger signal

→ Thus, the monostable multivibrator has one, quasi stable state and one stable state i.e it returns Quasi-to-stable by applying -ve trigger pulse at the I/P of differentiator & Diode 'D_2', & it will produce -ve spike which is applied to +ve I/P So, the voltage at +ve I/P is < 0.7 So, the O/P switches to $-V_{sat}$. & when the capacitor 'C' discharges to $-\beta V_{sat}$, again the O/P switches back to '$+V_{sat}$' & then capacitor again charges & clamped to 0.7V. At this stage, the O/P stay permanently at "$+V_{sat}$" until again another triggerpulse is applied.

→ Now, we have to calculate the pulse-width 'T' of monostable multivibrator as,

$$V_C = V_f + (V_i - V_f)\, e^{-t/RC}$$

Where, V_i → is the initial value, $V_C = V_D$.

V_f → is the final value of V_C = $-V_{sat}$. (forward diode voltage)

$$\therefore \quad V_C = -V_{sat} + (V_D + V_{sat})\, e^{-t/RC}$$

At time, $t = T$

$$V_C = -\beta V_{sat}$$

$$\therefore -\beta V_{sat} = -V_{sat} + (V_D + V_{sat})\, e^{-T/RC}$$

$$\Rightarrow V_{sat}(1-\beta) = (V_D + V_{sat})\, e^{-T/RC}$$

$$\therefore T = RC \ln\left(\frac{1 + \frac{V_D}{V_{sat}}}{1-\beta}\right)$$

where $\beta = \frac{R_2}{R_1 + R_2}$

If $V_{sat} >> V_D$, & $R_1 = R_2$ so, $\beta = 0.5$

$$\therefore T = 0.69RC$$

→ For monostable operation, the trigger pulse width 'T_P' should be much less than 'T', i.e the pulse width of O/P of monostable multivibrator

→ The diode 'D2' in the ckt is used to avoid the -ve spikes from the differentiator.

* The monostable multivibrator ckt is also referred to as "time delay ckt", as it generates a fast transition at a predetermined time 'T' after the application of i/p trigger.

* It is also called a "gating ckt", as it generates a rectangular waveform at a definite time & thus could be used to gate parts of a system.

IC 555 Timer.

The Astable & monostable ckts, so far we have seen, are, so commonly required that, special-monolithic IC's, called "IC timers," have been made available. One ex:- is "IC 555 timer", which has a wide acceptance in terms of cost & versatility.

→ The 555 timer is a highly stable device for generating accurate "time delay" (or) "oscillation". It was first introduced by "Signetic Corporation", as "SE/NE 555" & it is available in two package styles i.e. "8-pin Circular type", "TO-99 can", (or) 8-pin mini-DIP, (or) as "14 pin DIP". The 556 timer contains two 555 timers & is a 14-pin DIP.

→ There is also available Counter timer such as "Exar's XR-2240" which contains a "555 timer plus a" programmable binary Counter" in a single 16-pin package.

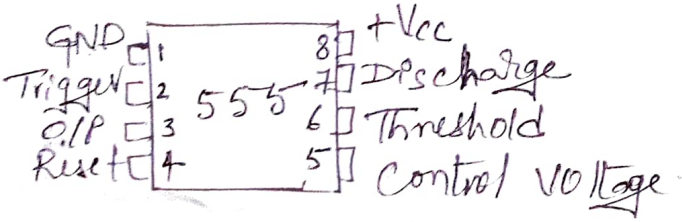
→ A single 555 timer can provide time delay ranging from "μs" to "hrs", where as timer can be used for max: timing range of days.

→ The "SE-555 timer" is designed for the operating temp: range from -55° to $+125^{\circ}C$, while the "NE-555 timer" operates over a temp: range of "0° to $70^{\circ}C$". The important features of the NE-555 timers are:

- → Operation on +5 to +18V supply voltage in both astable & monostable mode.
- → Adjustable duty cycle.
- → Timing from μsec to hrs.
- → High current o/p
- → Capacity to source (or) sink current of 200mA.
- → o/p can drive TTL & CMOS
- → Temp. stability of 50 part per million (ppm)/°C change in temp: (or) 0.005% per °C
- → Reliable, Easy to use, & low cost like a general purpose op-amp.
- → Since, it is easy to use, it used in applications, oscillator, pulse generator, ramp & square wave generator, mono-shot multivibrator, traffic light control & voltage monitor & burglar alarm.

Pin diagram of 555 timer:

Now Let us see the pin diagram of 555 timer shown below.



→ The above pin diagram is for 8-pin DIP (8) & 8 pin metal can packages. Now, let us see the description each pin.

Pin-1: Ground. All voltages are measured w.r.to GND.

Pin-2: Trigger: The o/p of the timer depends on the amplitude of the external trigger pulse applied to this pin.

pin-3: o/p: There are two ways, a load can be connected to the o/p terminal. Either b/w o/p & GND, (or) b/w, o/p-supply +Vcc

* when the o/p is Low, the load current passes through the load which is connected b/w o/p & +Vcc & the current passing into o/p is called "sink current" & that load is called "normally on load".

* when the o/p is high, o/p supplies current to the load connected b/w o/p & GND is called "normally off load" & that current is called "source current".

* The max: value of source (or) sink current is 200mA

Pin-4 : Reset : The 555 timer is "reset" or disabled by applying a "-ve pulse" to this pin, & when the reset pin is not in use, that terminal should be connected to +Vcc to avoid any "false triggering"

pin 5 : Control voltage :- An external voltage applied to this terminal changes the threshold as well as the "trigger voltage". When it is not used, it should be bypassed to GND with a 0.01μF capacitor to prevent any noise disturbances.

pin-6 : Threshold : This is the non-inverting terminal of comparator 'C', which monitors the voltage across the external capacitor. When the voltage at this pin is $\geq \frac{2Vcc}{3}$, the o/p of comparator 'C' goes "high", which in turn switches the o/p of the timer low

pin-7 : Discharge :- This pin is internally connected to the collector of transistor 'Q_1'. In functional diagram, when the o/p is high, the Q_1 "off" & acts as open ckt. to the external capacitor connected b/w. pin-7 & GND. On the other hand when o/p → low, Q_1 → saturated & acts as a short ckt, shorting out the external capacitor to GND

pin-8 : +Vcc : The supply voltage of +5V to +18V is applied to this pin w.r.to gnd

Functional diagram of 555 timer:-

→ The below fig. shows the functional blockdiagram of 555 timer

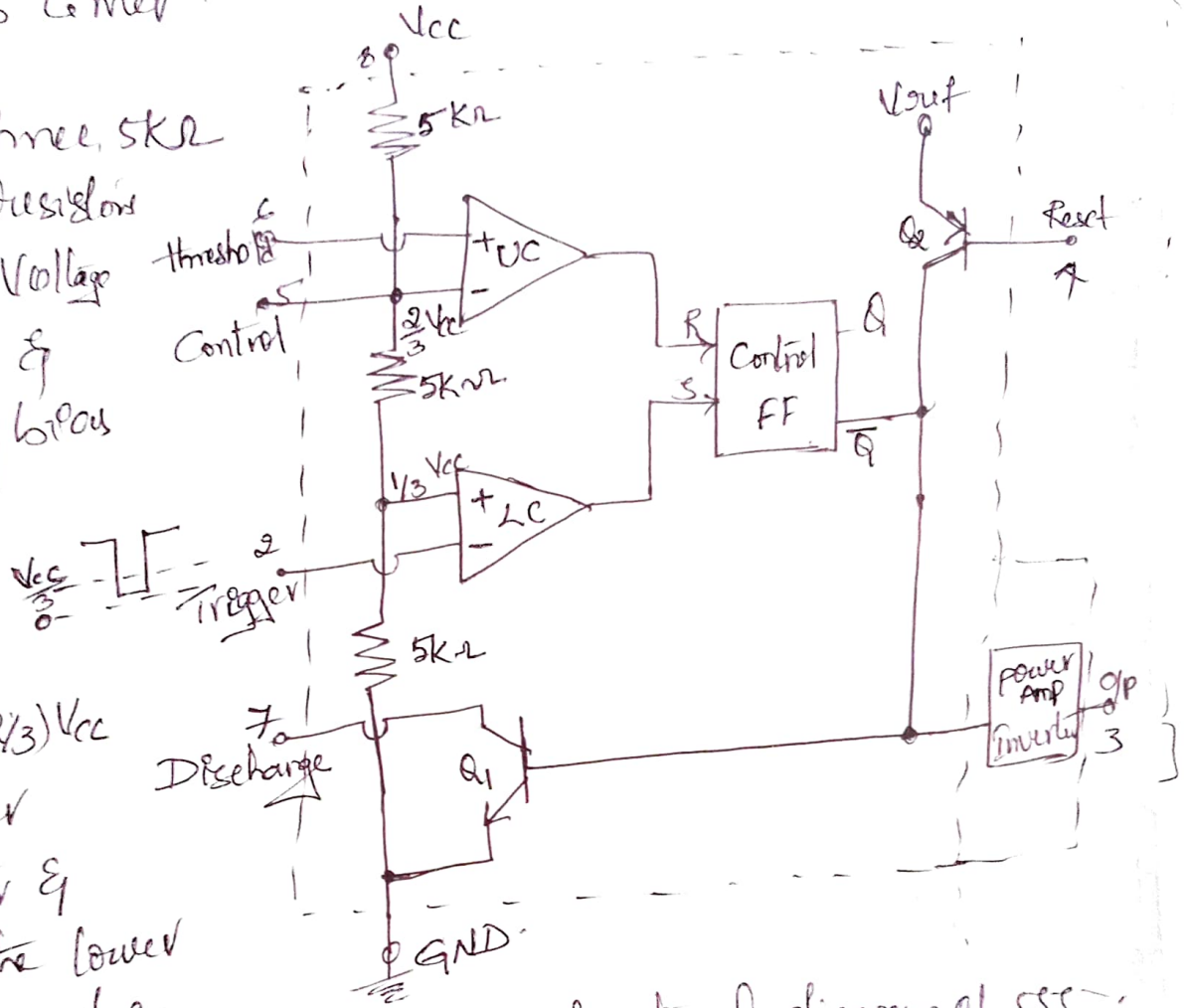


fig. functional diagram of 555

→ Here, three 5KΩ internal resistors acts as voltage divider, & providing bias voltage of (2/3)Vcc to the upper comparator & (1/3)Vcc to the lower comparator. where,

Vcc → supply voltage

→ since, these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval.

→ It is possible to vary time electronically too, by applying a modulation voltage to the control voltage i/p terminal (pin 5).

→ In applications, where no such modulation is intended, it is recommended by the manufacturers that, a capacitor (0.01 μF) be connected b/w Control voltage terminal (5) & GND to bypass "noise" (or) "ripple" from the supply.

→ In the stand by (stable) state, the O/P $\overline{Q}$ of the Control Flip Flop FF is "High". This makes the O/P "Low", because of power amp: which is basically an inverter.

→ A -ve going triggering pulse is applied to pin-2 & should have its d.c level greater than the threshold level of the lower comparator (i.e $\frac{V_{cc}}{3}$).

→ At the -ve going edge of the trigger, as the trigger passes through "$\frac{V_{cc}}{3}$", the O/P of the Lower Comparator goes "High". & "sets" the FF. i.e $Q=1$ & $\overline{Q}=0$.

→ During the +ve going edge, when the threshold voltage at pin-6 passes through $(\frac{2}{3})V_{cc}$, the O/P of Upper Comparator goes "High". & resets the FF i.e $Q=0$ & $\overline{Q}=1$

→ The reset i/p (pin 4) provides a mechanism to reset the FF in a manner which ~~provides~~ overrides the effect of any instruction coming to FF from the Lower Comparator. This overriding reset is effective when the reset i/p is less than about 0.4V.

→ This overriding reset is effective when the reset i/p is less than about 0.4V. When this reset is not used, it is returned to "Vcc". (10)

→ The transistor 'Q' serves as a buffer to isolate the reset o/p from the "FF" & transistor 'Q'. The transistor 'Q' is driven by an internal reference voltage 'Vref' obtained from the supply voltage "Vcc".

Monostable operation using 555 timer :-

→ First of all Let we see the IC 555 timer, connected as monostable multivibrator as shown below.

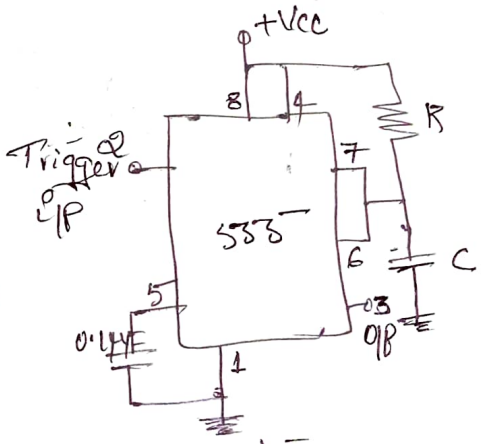


fig : 555 timer as monostable multivibrator

→ Next Let we see the functional diagram of 555 timer as monostable inorder to know the operation

→ In the standby state, the flipflop holds the transistor Q_1 → ON, thus clamping the external timing capacitor 'c' to ground.

→ The o/p remains at ground potential i.e Low. As the trigger passes through $\frac{V_{cc}}{3}$, then the FF is set i.e $\overline{Q} = 0$. This makes the transistor Q_1 → OFF, & the short ckt across the 'c' is released

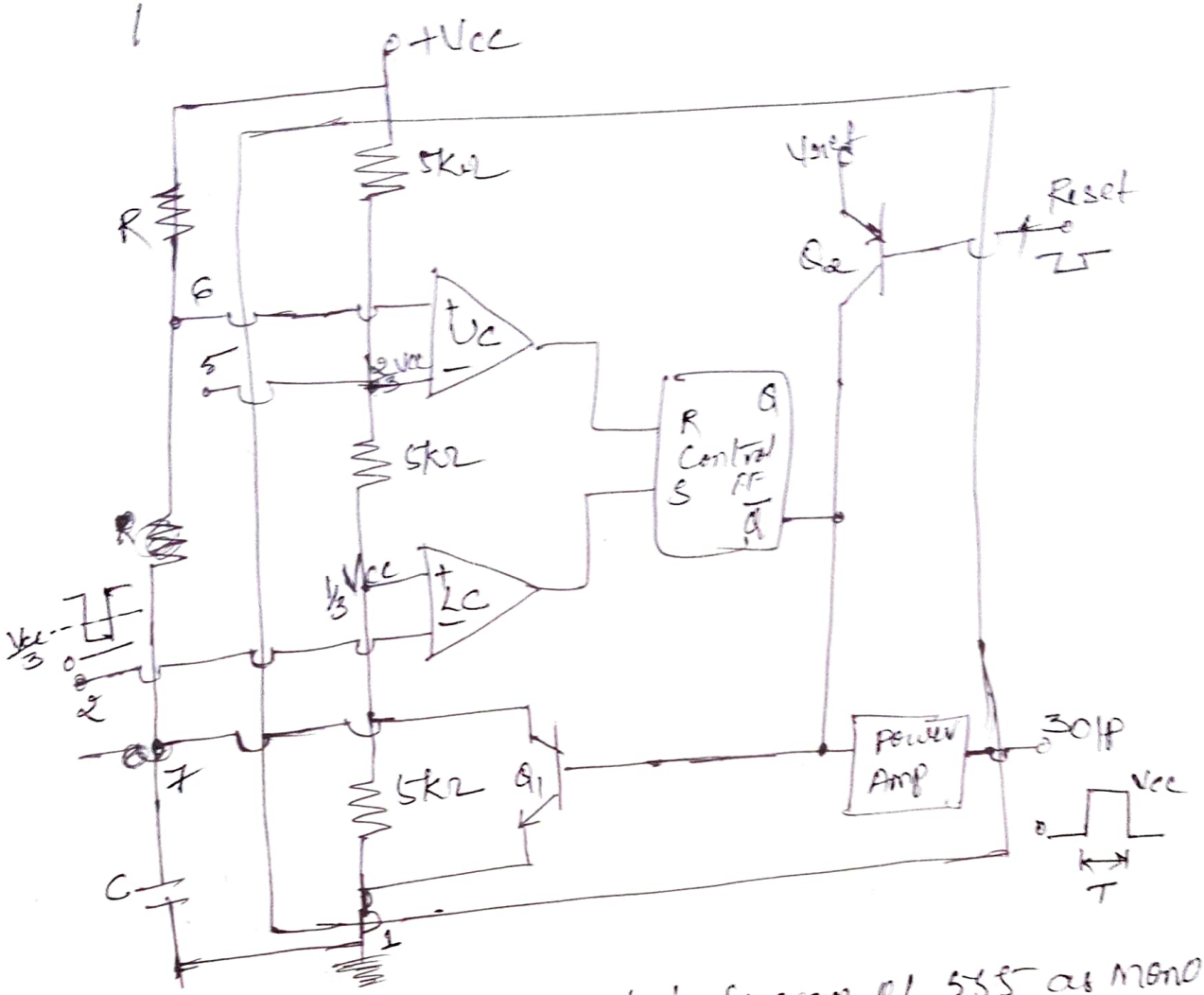
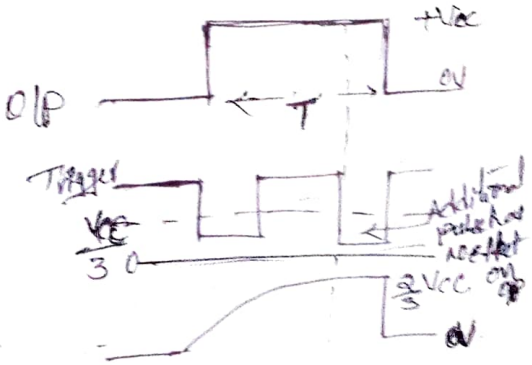


fig:- function Block diagram of 555 as mono-stable multi

→ As $\overline{Q}$ is Low, means the o/p goes high (≈ Vcc). The timing cycle now begins. Since the capacitor 'C' is Unclamped, the voltage across it rises exponentially through 'R' towards 'Vcc' with a time Constant = RC" as shown in fig.

→ After a time period 'T', the capacitor voltage is just greater (or) Equal $\frac{2}{3}$ Vcc, the Upper comparator will Reset the FF.



→ that is, R=1, S=0. So, this makes $\bar{Q}=1$, so the transistor 'Q_1' goes ON (i.e saturates), thereby discharging the capacitor 'C', rapidly to gnd potential as shown in the o/p fig:

→ Now, Let we Calculate the voltage across the capacitor, is given by $V_c(t) = V_f + (V_i - V_f)e^{-t/RC}$

$$V_c = V_{cc}(1 - e^{-t/RC})$$

$V_i \to 0$
$V_f \to V_{cc}$

At $t = T \Rightarrow V_c = \frac{2}{3}V_{cc}$

$$\therefore \frac{2}{3}V_{cc} = V_{cc}(1 - e^{-T/RC})$$

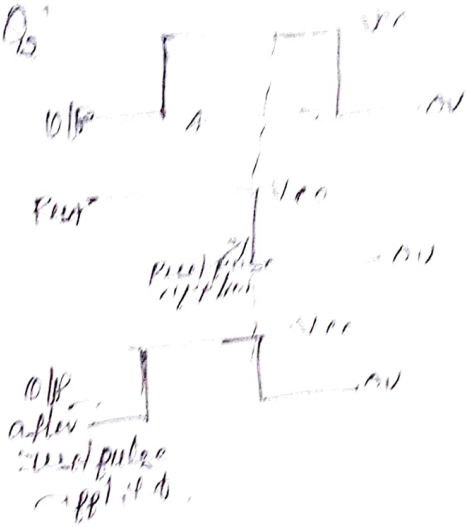
$$\therefore T = RC \ln(1/3)$$

$$= 1.1\ RC \text{ (sec's)}$$

→ From the above Eq:, we can say that, the timing interval is independent of the supply voltage. It may also be noted that, once triggered, the o/p remain in 'high' state until the time 'T' elapses, which depends only on 'R' & 'C'.

→ Any additional trigger pulse comming during this time will not change the o/p state. However, if a reset pulse is applied to the reset terminal, i.e. pin 4., during the timing cycle, transistor 'Q_2' → off, Q_1 becomes on & the external timing capacitor 'C' is immediately discharged

→ Now, the o/p will be reversed as shown in fig.
As shown in the fig:, the o/p of Q_2 is directly connected to the i/p of Q_1 so as to turn on Q_1 immediately & thereby avoid the propagation delay through the F.F.



→ Now, even if the trigger is released, the o/p will still remain "LOW" until a +ve going trigger pulse is again applied at pin 2.

→ Sometimes, the monostable of this type will misfire/trigger on +ve pulse edges, even with the control pin is bypassed via the capacitor. So, to prevent this, the ckt is modified by placing a resistor and capacitor combination of 10kΩ & 0.001 μF at the i/p forms a differentiator. as shown in fig:

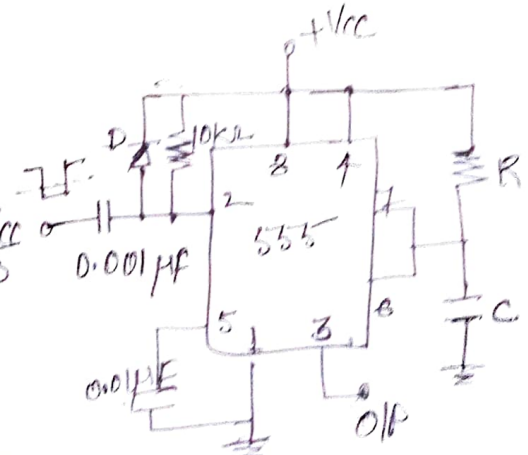


fig: modified monostable.

→ During the +ve going edge of the trigger, the diode D becomes forward biased, thereby limiting the amplitude of the +ve spike to 0.7V.

Applications → pulse width modulation, → Linear Ramp generator, → Freq: divider

Astable operation Using 555 timer :-

→ The ckt, connected as Astable using 555 timer is shown in fig:

→ In order to understand the operation, Let we see the function diagram of astable as shown in below fig:

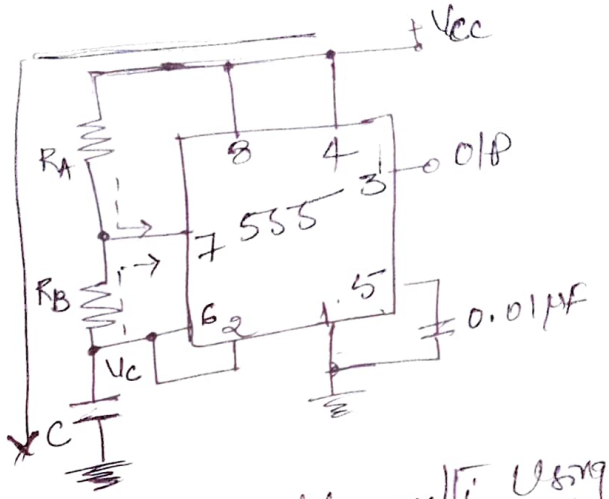


fig. Astable multi Using 555 timer

→ Compared to monostable operation, there, no trigger is needed, so, the pin 2 is connected to gnd via the capacitor 'C', & the timing resistor 'R' is divided into 'RA' & 'RB'. also Compared to monostable, here, as shown below in above fig

→ The pin '7' of discharging transistor 'Q1' is connected to the junction of RA & RB. When the power supply 'Vcc' is connected, the External timing Capacitor 'C' charges towards 'Vcc' with a time Constant (RA+RB)C

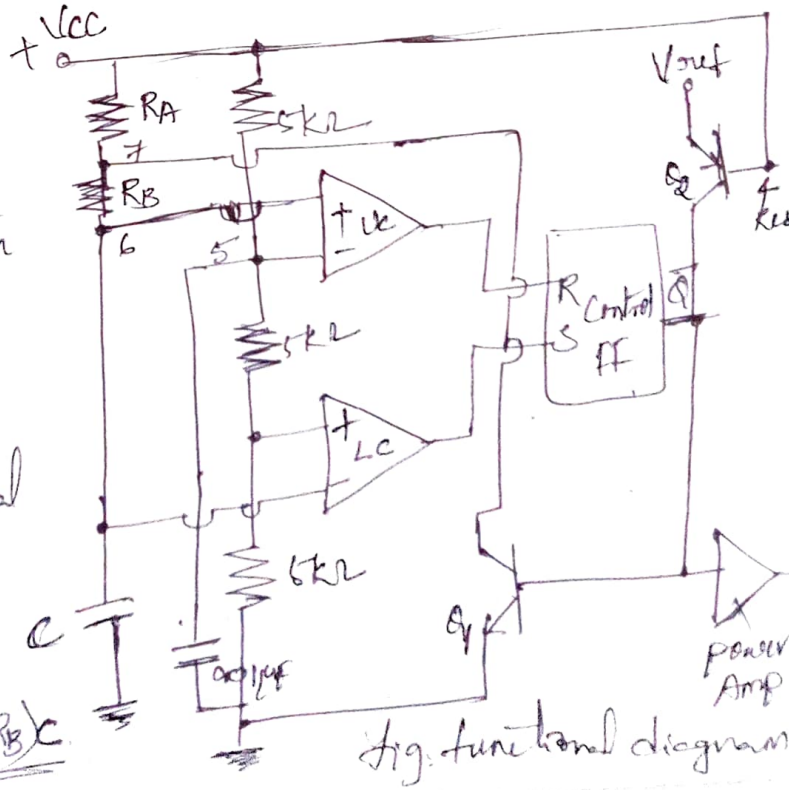


fig. functional diagram

→ During this time, the o/p pin is "high" (≈ V_{cc}) as Reset R=0, & S=1 & this combination makes $\bar{Q}=0$ which will unclamps the timing capacitor 'C' (or) release the shortckt.

→ When the voltage across the capacitor, Equal (or) to be precise is just greater than $\frac{2}{3}V_{cc}$; the upper comparator triggers the FF so that, $\bar{Q}=1$. This is in turn makes transistor 'Q_1' → ON & the capacitor starts discharges towards gnd & through 'R_B' & transistor 'Q_1'. with a time constant "$R_B \cdot C$".

→ Why because, the current flows into transistor 'Q_1' through 'R_A'. The resistors 'R_A' & 'R_B' must be large Enough to limit this current & prevent damage to the discharge transistor 'Q_1'. The min: value of 'R_A' is approx: Equal to $\frac{V_{cc}}{0.2}$, where '0.2A' is the max: current flows through transistor 'Q_1' when it is ON.

→ During the discharge of the timing capacitor 'C' as it reaches (to be precise, is just less than) $\frac{V_{cc}}{3}$, the lower comparator is triggered & makes. S=1 & R=0, which turns $\bar{Q}=0$., which turn off unclamps the External timing capacitor 'C', so, it charges to $\frac{2}{3}V_{cc}$. Thus, the capacitor periodically changed & discharged b/w $\frac{2}{3}V_{cc}$ & $\frac{1}{3}V_{cc}$ respectively as shown in fig.

→ The fig: shows the timing seq: of o/p of astable

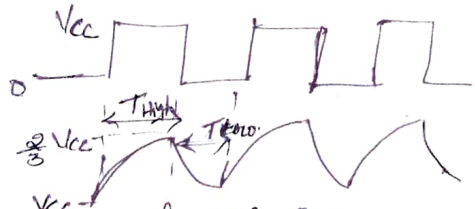


fig. Timing seq:

A3, A5, M4, A6, 9, 11, 14, 23

multi & as well as the capacitor voltage waveform which is a sawtooth.

(13)

→ When the O/P is "high" & the time taken by the capacitor to change from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$. It is known as 't_{high}'

→ While the O/P is "low", & the time taken by the capacitor to discharge from $\frac{2}{3}V_{cc}$ to $\frac{1}{3}V_{cc}$ is known as "t_{low}".

→ First of all, Let we Calculate, 't_H'.

the voltage across capacitor 'C' is,

$$V_c = V_{cc}(1-e^{-t/RC})$$

Let we denote, the time taken by the ckt to change from 0 to $\frac{2}{3}V_{cc}$ is,

$$\frac{2}{3}V_{cc} = V_{cc}(1-e^{-t_1/RC})$$

$$\therefore t_1 = 1.09RC$$

Let we denote the time taken by the ckt to change from 0 to $\frac{1}{3}V_{cc}$ is,

$$\frac{1}{3}V_{cc} = V_{cc}(1-e^{-t_2/RC})$$

$$t_2 = 0.405RC$$

→ So, the time to change from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$ is

$$t_{High} = t_1 - t_2$$
$$= 1.09RC - 0.405 = 0.69RC$$

So, for the given ckt, the capacitor charges through $(R_A+R_B)C$.

$$\boxed{t_{High} = 0.69(R_A+R_B)C}$$

→ Now, Let we calculate, t_{LOW}, i.e. from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$

$$\frac{1}{3}V_{CC} = \frac{2}{3}V_{CC}\, e^{-t/RC}$$

$$t = 0.69RC$$

→ So, for the given ckt, the capacitor discharges through $R_B C$ ∴ $\boxed{t_{LOW} = 0.69 R_B C}$

Therefore, the total time, $T = T_{HIGH} + T_{LOW}$

$$= 0.69(R_A + 2R_B)C$$

$$\therefore f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

* Duty cycle :- is defined as the ratio of 'ON' time to the total time period T ($t_{HIGH} + t_{LOW}$). Here, in this ckt, when the transistor 'Q_1' is ON, the O/P goes low

Hence,

$$\%\text{ Duty cycle} = \frac{t_{ON}}{T} \times 100 = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

→ Therefore, in this configuration, it is not possible to have a duty cycle more than 50%. Since, $t_{HIGH} = 0.69(R_A + R_B)C$ will always > $t_{LOW} = 0.69 R_B C$.

→ In-order to obtain a symmetrical square wave, i.e D = 50%, the resistance 'R_A' must be reduced to zero. However, now pin 7 is connected directly to 'V_{CC}' & extra current will flow through 'Q_1' when it is 'ON'. This may damage 'Q_1' as well as timer ckt.

→ An alternative ckt, which will allow duty cycle to be set at practically any level is shown in below fig:

→ As shown in fig:, During the charging portion of the cycle, diode 'D1' is forward biased effectively short circuiting 'RB'.

So that, $t_{HIGH} = 0.69 R_A \cdot C$

→ However, during the discharging portion of the cycle, the transistor 'Q1' becomes 'ON', thereby grounding pin-7, & hence the diode 'D1' is reverse biased, So,

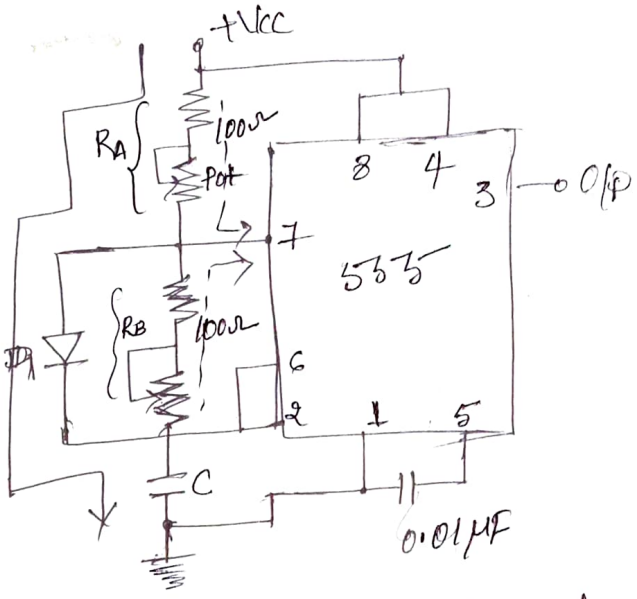


fig: Adjustable duty cycle rectangular wave generator

$$t_{LOW} = 0.69 R_B \cdot C$$

$$\therefore T = t_{HIGH} + t_{LOW}$$

$$= 0.69 (R_A + R_B) C$$

$$\therefore f = \frac{1.45}{(R_A + R_B) C}$$

$$\therefore \text{Duty cycle, } D = \frac{R_B}{R_A + R_B}$$

→ Here, the resistors 'R_A' & 'R_B' could be made variable to allow the adjustment of freq. & pulse width. However, a series resistor of atleast 100Ω (fixed) should be added to each 'R_A' & 'R_B'. This will limit, the peak current to the discharge transistor 'Q_1', when the variable resistors are at minimum value.

→ And if, 'R_A' is made equal to 'R_B', then 50% of duty-cycle is achieved.