II B. TECH I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	TOTAL CREDITS
	3	0	**0**	30	70	100	3
SUB CODE: R23EC2104	**ELECTRONICS DEVICES AND CIRCUITS**						

COURSE OBJECTIVES:

1. Understand the operation and principles of P-N diode.
2. Understand various types of Special diodes, rectifiers and filters.
3. Know the working of BJT.
4. Know the need for transistor biasing and stabilization.
5. Know the working of FET and other Transistors.

COURSE OUTCOMES:

After completion of the course, students will be able to

CO1: Use P-N diodes in electronic circuits.

CO2: Use special diodes and rectifiers in electronic circuits.

CO3: Explore the operation of BJT and its applications.

CO4: Analyze the thermal stability of BJT.

CO5: Explore the operation of FET, other transistors and their applications.

SYLLABUS:

UNIT- I: PN JUNCTION DIODE CHARACTERISTICS:

Insulators, Semiconductors and Metals–Classification using Energy gap, Intrinsic and Extrinsic Semiconductors. P-N Junction Diode - Formation of P-N Junction, Open Circuited P-N Junction, Biased P-N Junction - Forward Bias, Reverse Bias, Current Components in PN Junction Diode, Law of Junction, Diode Current Equation - Quantitative Analysis, V-I Characteristics of Diode - Forward Bias, Reverse Bias, Breakdown in P-N Junction Diode, Temperature Dependence on V-I Characteristics, Diode Resistance-Static Resistance, Dynamic Resistance, Reverse Resistance, Diode Capacitance - Transition Capacitance, Diffusion Capacitance, Energy Band Diagram of PN Junction Diode.

UNIT- II: SPECIAL DIODES AND DIODE CIRCUITS:

SPECIAL DIODES:

Zener Diode - V-I Characteristics, Applications, Breakdown Mechanisms - Zener Breakdown and Avalanche Breakdown, Construction, Operation, Characteristics and applications of LED, LCD, Photodiode, Varactor Diode and Tunnel diode.

DIODE CIRCUITS: Clipping (limiting) circuits, Clipping at Two Independent Levels, Peak Detector, Clamping circuits, Basic Rectifier setup, Half Wave Rectifier, Full Wave Rectifier,

Bridge Rectifier, Inductive and Capacitive Filters, L– Section and π- Section, Derive and compare rectifier parameters with and without filter.

UNIT- III: BIPOLAR JUNCTION TRANSISTOR (BJT):

Bipolar Junction Transistor – Types, Symbols and Operation, Transistor Current Components, Transistor Equation - Relation among I_C, I_B, I_{CBO}, Transistor Configurations - CB, CE and CC, Transistor as a switch, Transistor switching times, Transistor as an Amplifier, Characteristics of Transistor in Common Base Configuration, Common Emitter and Common Collector Configurations - Input and output characteristics, Early effect, Transistor parameters, Current amplification factor, Relation among α, β, and γ, Comparison of CB, CE and CC Configurations, Punch Through/ Reach through, Typical transistor junction voltage values, Photo Transistor.

UNIT- IV: BJT BIASING AND THERMAL STABILITY:

Need For Biasing, Operating Point, Load Line Analysis - D.C. Load Line, A.C. Load Line, Biasing - Methods, Basic Stability, Fixed Bias, Collector-to-base Bias and Self Bias, Stabilization against variations in VBE, Ic and β, Stability Factors S, S' and S'', Bias Compensation - Thermistor, Sensistor, Diode Compensation for variation in ICO, Thermal Runaway, Thermal Stability.

UNIT- V: FET & OTHER TRANSISTORS:

FET Types and Symbols - JFET and MOSFET/IGFET, JFET: N- Channel and P-Channel Construction, Operation, Characteristics - Drain and Transfer, Parameters - Drain Resistance, Amplification factor, Transconductance, Pinch-off voltage, MOSFET - Types - Depletion MOSFET - N Channel and P Channel, Enhancement MOSFET - N-Channel and P-Channel, Construction, Operation, Characteristics - Transfer and Drain Characteristics for Depletion and Enhancement Modes , Analysis of MOSFETs, Comparison between JFET and MOSFET.

SCR- Symbol, Two-Transistor version, UJT - Negative Resistance Property and Applications.

TEXT BOOKS:

1. J. Millman, C. Halkias, "Electronic Devices and Circuits", Tata McGraw-Hill, Third edition, 2010.
2. Allen Mottershed, "Electronic Devices and Circuits", PHI, 2011.
3. Salivahanan, N. Suresh Kumar, A. Vallavaraj, "Electronic Devices and Circuits" Tata McGraw-Hill, Second Edition, 2008.

REFERENCE BOOKS:

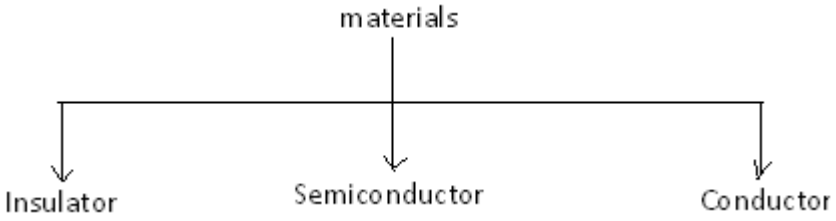
1. Jacob Millman, C. Halkies, C.D. Parikh, Satyabrata Jit, "Integrated Electronics", Tata McGraw-Hill, Second Edition, 2011.
2. R.L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuit Theory", Pearson Publications, Eleventh Edition, 2013

UNIT 1

SEMICONDUCTOR PHYSICS

1.0 INTRODUCTON

Based on the electrical conductivity all the materials in nature are classified as insulators, semiconductors, and conductors.



Insulator: An insulator is a material that offers a very low level (or negligible) of conductivity when voltage is applied. Eg: Paper, Mica, glass, quartz. Typical resistivity level of an insulator is of the order of 10^{10} to 10^{12} Ω-cm. The energy band structure of an insulator is shown in the fig.1.1. Band structure of a material defines the band of energy levels that an electron can occupy. Valance band is the range of electron energy where the electron remain bended too the atom and do not contribute to the electric current. Conduction bend is the range of electron energies higher than valance band where electrons are free to accelerate under the influence of external voltage source resulting in the flow of charge.

The energy band between the valance band and conduction band is called as forbidden band gap. It is the energy required by an electron to move from balance band to conduction band i.e. the energy required for a valance electron to become a free electron.

$$1 \text{ eV} = 1.6 \times 10^{-19} \text{ J}$$

For an insulator, as shown in the fig.1.1 there is a large forbidden band gap of greater than 5Ev. Because of this large gap there a very few electrons in the CB and hence the conductivity of insulator is poor. Even an increase in temperature or applied electric field is insufficient to transfer electrons from VB to CB.

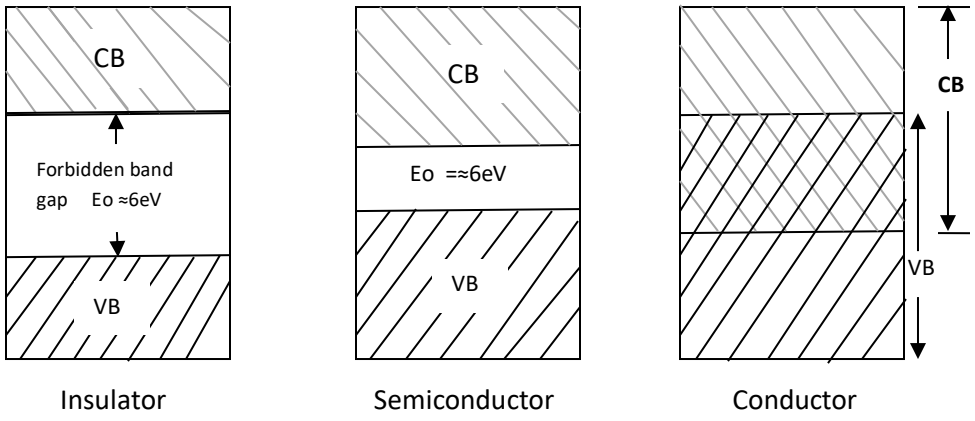


FiG:1.1 Energy band diagrams insulator, semiconductor and conductor

Conductors: A conductor is a material which supports a generous flow of charge when a voltage is applied across its terminals. i.e. it has very high conductivity. Eg: Copper, Aluminum, Silver, Gold. The resistivity of a conductor is in the order of 10^{-4} and 10^{-6} Ω-cm. The Valance and conduction bands overlap (fig1.1) and there is no energy gap for the electrons to move from valance band to conduction band. This implies that there are free electrons in CB even at absolute zero temperature (0K). Therefore at room temperature when electric field is applied large current flows through the conductor.

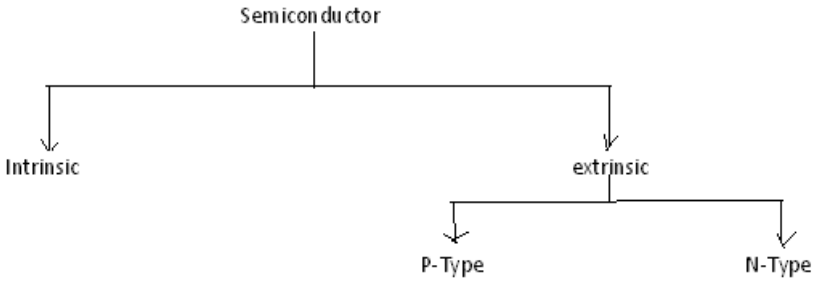
Semiconductor: A semiconductor is a material that has its conductivity somewhere between the insulator and conductor. The resistivity level is in the range of 10 and 10^4 Ω-cm. Two of the most commonly used are Silicon (Si=14 atomic no.) and germanium (Ge=32 atomic no.). Both have 4 valance electrons. The forbidden band gap is in the order of 1eV. For eg., the band gap energy for Si, Ge and GaAs is 1.21, 0.785 and 1.42 eV, respectively at absolute zero temperature (0K). At 0K and at low temperatures, the valance band electrons do not have sufficient energy to move from V to CB. Thus semiconductors act a insulators at 0K. as the temperature increases, a large number of valance electrons acquire sufficient energy to leave the VB, cross the forbidden bandgap and reach CB. These are now free electrons as they can move freely under the influence of electric field. At room temperature there are sufficient electrons in the CB and hence the semiconductor is capable of conducting some current at room temperature.

Inversely related to the conductivity of a material is its resistance to the flow of charge or current. Typical resistivity values for various materials are given as follows.

Insulator	Semiconductor	Conductor
10^{-6} Ω-cm (Cu)	50Ω-cm (Ge)	10^{12} Ω-cm (mica)
	$50x10^3$ Ω-cm (Si)	

Typical resistivity values

1.0.1 Semiconductor Types



A pure form of semiconductors is called as intrinsic semiconductor. Conduction in intrinsic sc is either due to thermal excitation or crystal defects. Si and Ge are the two most important semiconductors used. Other examples include Gallium arsenide GaAs, Indium Antimonide (InSb) etc.

Let us consider the structure of Si. A Si atomic no. is 14 and it has 4 valance electrons. These 4 electrons are shared by four neighboring atoms in the crystal structure by means of covalent bond. Fig. 1.2a shows the crystal structure of Si at absolute zero temperature (0K). Hence a pure SC acts has poor conductivity (due to lack of free electrons) at low or absolute zero temperature.

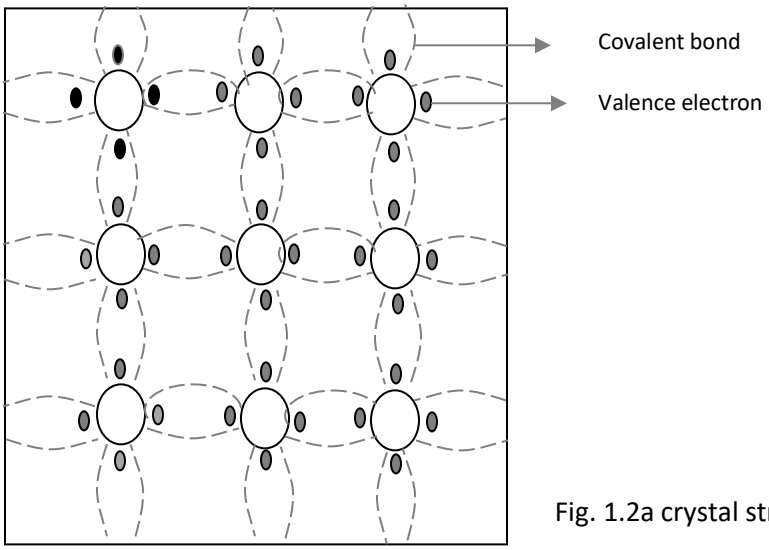


Fig. 1.2a crystal structure of Si at 0K

At room temperature some of the covalent bonds break up to thermal energy as shown in fig 1.2b. The valance electrons that jump into conduction band are called as free electrons that are available for conduction.

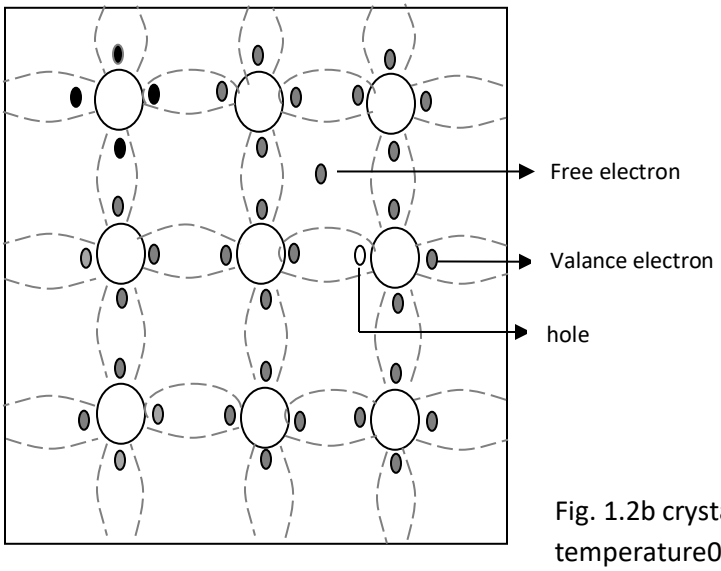
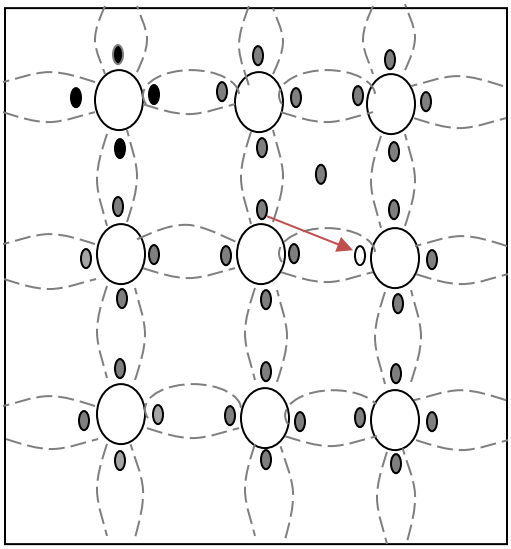


Fig. 1.2b crystal structure of Si at room temperature0K

The absence of electrons in covalent bond is represented by a small circle usually referred to as hole which is of positive charge. Even a hole serves as carrier of electricity in a manner similar to that of free electron.

The mechanism by which a hole contributes to conductivity is explained as follows:

When a bond is in complete so that a hole exists, it is relatively easy for a valance electron in the neighboring atom to leave its covalent bond to fill this hole. An electron moving from a bond to fill a hole moves in a direction opposite to that of the electron. This hole, in its new position may now be filled by an electron from another covalent bond and the hole will correspondingly move one more step in the direction opposite to the motion of electron. Here we have a mechanism for conduction of electricity which does not involve free electrons. This phenomenon is illustrated in fig1.3



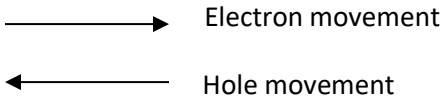


Fig. 1.3a

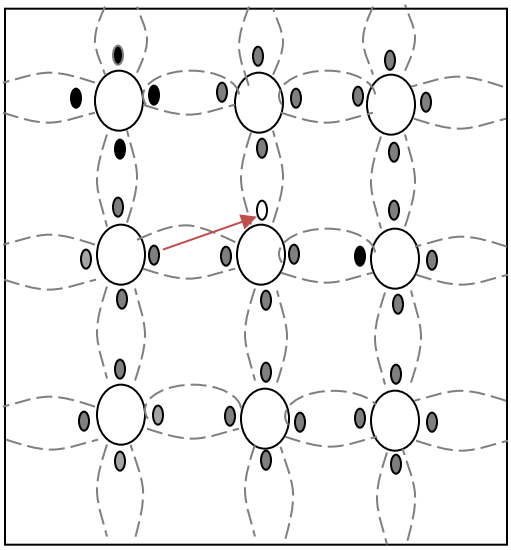


Fig. 1.3b

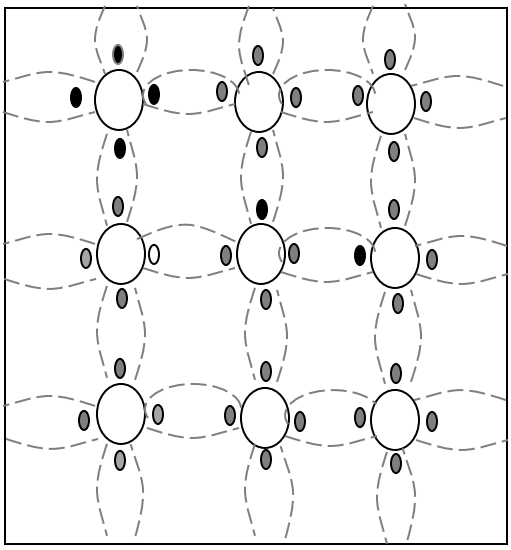


Fig. 1.3c

Fig 1.3a show that there is a hole at ion 6.Imagine that an electron from ion 5 moves into the hole at ion 6 so that the configuration of 1.3b results. If we compare both fig1.3a &fig 1.3b, it appears as if the hole has moved towards the left from ion6 to ion 5. Further if we compare fig 1.3b and fig 1.3c, the hole moves from ion5 to ion 4. This discussion indicates the motion of hole is in a direction opposite to that of motion of electron. Hence we consider holes as physical entities whose movement constitutes flow of current.

In a pure semiconductor, the number of holes is equal to the number of free electrons.

1.0.2 EXTRINSIC SEMICONDUCTOR:

Intrinsic semiconductor has very limited applications as they conduct very small amounts of current at room temperature. The current conduction capability of intrinsic semiconductor can be increased significantly by adding a small amounts impurity to the intrinsic semiconductor. By adding impurities, it becomes impure or extrinsic semiconductor. This process of adding impurities is called as doping. The amount of impurity added is 1 part in 10^6 atoms.

N type semiconductor: If the added impurity is a pentavalent atom then the resultant semiconductor is called N-type semiconductor. Examples of pentavalent impurities are Phosphorus, Arsenic, Bismuth, Antimony etc.

A pentavalent impurity has five valance electrons. Fig 1.3a shows the crystal structure of N-type semiconductor material where four out of five valance electrons of the impurity atom(antimony) forms covalent bond with the four intrinsic semiconductor atoms. The fifth electron is loosely bound to the impurity atom. This loosely bound electron can be easily

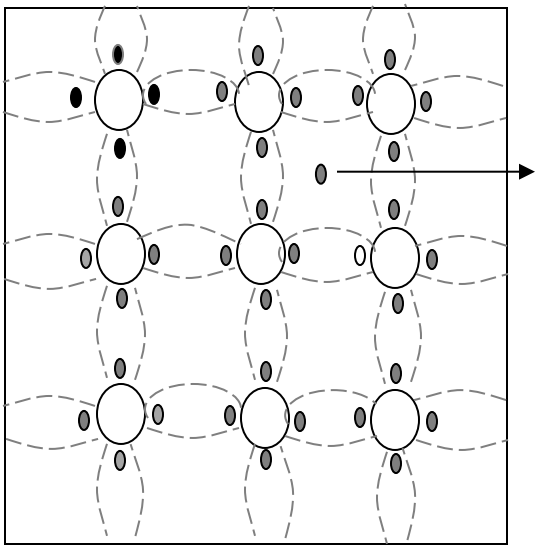


Fig. 1.3a crystal structure of N type SC

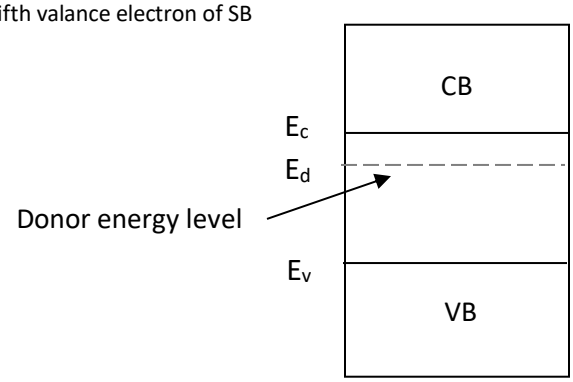


Fig. 1.3bEnergy band diagram of N type

excited from the valance band to the conduction band by the application of electric field or increasing the thermal energy. The energy required to detach the fifth electron form the impurity atom is very small of the order of 0.01ev for Ge and 0.05 eV for Si.

The effect of doping creates a discrete energy level called donor energy level in the forbidden band gap with energy level E_d slightly less than the conduction band (fig 1.3b). The difference between the energy levels of the conducting band and the donor energy level is the energy required to free the fifth valance electron (0.01 eV for Ge and 0.05 eV for Si). At room temperature almost all the fifth electrons from the donor impurity atom are raised to conduction band and hence the number of electrons in the conduction band increases significantly. Thus every antimony atom contributes to one conduction electron without creating a hole.

In the N-type sc the no. of electrons increases and the no. of holes decreases compared to those available in an intrinsic sc. The reason for decrease in the no. of holes is that the larger no. of electrons present increases the recombination of electrons with holes. Thus current in N type sc is dominated by electrons which are referred to as majority carriers. Holes are the minority carriers in N type sc

P type semiconductor: If the added impurity is a trivalent atom, then the resultant semiconductor is called P-type semiconductor. Examples of trivalent impurities are Boron, Gallium, indium etc.

The crystal structure of p type sc is shown in the fig1.3c. The three valance electrons of the impurity (boon) forms three covalent bonds with the neighboring atoms and a vacancy exists in

the fourth bond giving rise to the holes. The hole is ready to accept an electron from the neighboring atoms. Each trivalent atom contributes to one hole generation and thus introduces a large no. of holes in the valance band. At the same time the no. electrons are decreased compared to those available in intrinsic sc because of increased recombination due to creation of additional holes.

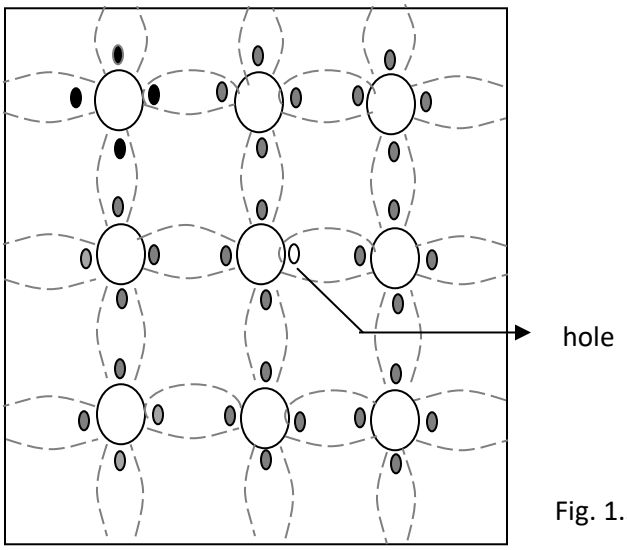


Fig. 1.3c crystal structure of P type sc

Thus in P type sc , holes are majority carriers and electrons are minority carriers. Since each trivalent impurity atoms are capable accepting an electron, these are called as acceptor atoms. The following fig 1.3d shows the pictorial representation of P type sc

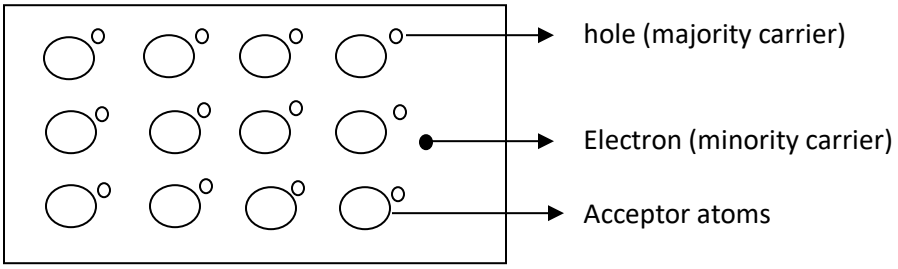


Fig. 1.3d crystal structure of P type sc

- The conductivity of N type sc is greater than that of P type sc as the mobility of electron is greater than that of hole.
- For the same level of doping in N type sc and P type sc, the conductivity of an Ntype sc is around twice that of a P type sc

1.0.3 CONDUCTIVITY OF SEMICONDUCTOR:

In a pure sc, the no. of holes is equal to the no. of electrons. Thermal agitation continue to produce new electron- hole pairs and the electron hole pairs disappear because of recombination. with each electron hole pair created , two charge carrying particles are formed . One is negative which is a free electron with mobility μ_n . The other is a positive i.e., hole with mobility μ_p . The electrons and hole move in opppsitte direction in a an electric field E, but since they are of opposite sign, the current due to each is in the same direction. Hence the total current density J within the intrinsic sc is given by

$J = J_n + J_p$

$=q\, n\, \mu_n E + q\, p\, \mu_p E$

$= (n\, \mu_n + p\, \mu_p) qE$

$=\sigma E$

Where n=no. of electrons / unit volume i.e., concentration of free electrons

P= no. of holes / unit volume i.e., concentration of holes

E=applied electric field strength, V/m

q= charge of electron or hole I n Coulombs

Hence, σ is the conductivity of sc which is equal to $(n\, \mu_n + p\, \mu_p)q$. he resistivity of sc is reciprocal of conductivity.

$P = 1/\sigma$

It is evident from the above equation that current density with in a sc is directly proportional to applied electric field E.

For pure sc, $n=p= n_i$ where n_i = intrinsic concentration. The value of n_i is given by

$n_i^2 = AT^3 \exp(-E_{GO}/KT)$

therefore, $J= n_i (\mu_n + \mu_p) q E$

Hence conductivity in intrinsic sc is $\sigma i= n_i (\mu_n + \mu_p) q$

Intrinsic conductivity increases at the rate of 5% per ^{o} C for Ge and 7% per ^{o} C for Si.

Conductivity in extrinsic sc (N Type and P Type):

The conductivity of intrinsic sc is given by $\sigma i = n_i (\mu_n + \mu_p) q = (n \mu_n + p \mu_p)q$

For N type , n>>p

Therefore $\sigma = q n \mu_n$

For P type ,p>>n

Therefore $\sigma = q p \mu_p$

1.0.4 FERMI LEVEL:

1.0.5 CHARGE DENSITIES IN P TYPE AND N TYPE SEMICONDUCTOR:

Mass Action Law:

Under thermal equilibrium for any semiconductor, the product of the no. of holes and the concentration of electrons is constant and is independent of amount of donor and acceptor impurity doping.

$n.p = n_i^2$

where n= eleetron concentration

p = hole concentration

n_i^2= intrinsic concentration

Hence in N type sc , as the no. of electrons increase the no. of holes decreases. Similarly in P type as the no. of holes increases the no. of electrons decreases. Thus the product is constant and is equal to n_i^2 in case of intrinsic as well as extrinsic sc.

The law of mass action has given the relationship between free electrons concentration and hole concentration. These concentrations are further related by the law of electrical neutrality as explained below.

Law of electrical neutrality:

Sc materials are electrically neutral. According to the law of electrical neutrality, in an electrically neutral material, the magnitude of positive charge concentration is equal to tat of negative charge concentration. Let us consider a sc that has N_D donor atoms per cubic centimeter and N_A acceptor atoms per cubic centimeter i.e., the concentration of donor and acceptor atoms are N_D and N_A respectively. Therefore N_D positively charged ions per cubic centimeter are

contributed by donor atoms and N_A negatively charged ions per cubic centimeter are contributed by the acceptor atoms. Let n, p is concentration of free electrons and holes respectively. Then according to the law of neutrality

$N_D + p = N_A + n$ ……eq 1.1

For N type sc, $N_A = 0$ and $n >> p$. Therefore $N_D \approx n$ ……eq 1.2

Hence for N type sc the free electron concentration is approximately equal to the concentration of donor atoms. In later applications since some confusion may arise as to which type of sc is under consideration a the given moment, the subscript n or p is added for Ntype or P type respectively. Hence eq1.2 becomes $N_D \approx n_n$

Therefore current density in N type sc is $J = N_D \mu_n q E$

And conductivity $\sigma = N_D \mu_n q$

For P type sc, $N_D = 0$ and $p >> n$. Therefore $N_A \approx p$

Or $N_A \approx p_p$

Hence for P type sc the hole concentration is approximately equal to the concentration of acceptor atoms.

Therefore current density in N type sc is $J = N_A \mu_p q E$

And conductivity $\sigma = N_A \mu_p q$

Mass action law for N type, $n_n p_n = n_i^2$

$p_n = n_i^2 / N_D$ since ($n_n \approx N_D$)

Mass action law for P type, $n_p p_p = n_i^2$

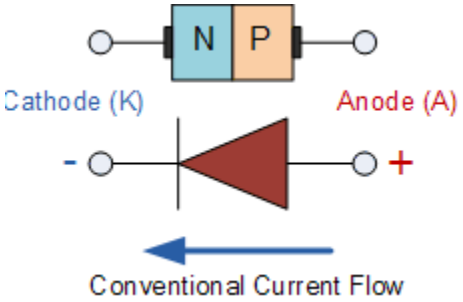
$n_p = n_i^2 / N_A$ since ($p_p \approx N_A$)

1.1 QUANTITATIVE THEORY OF PN JUNCTION DIODE:

1.1.1 PN JUNCTION WITH NO APPLIED VOLTAGE OR OPEN CIRCUIT CONDITION:

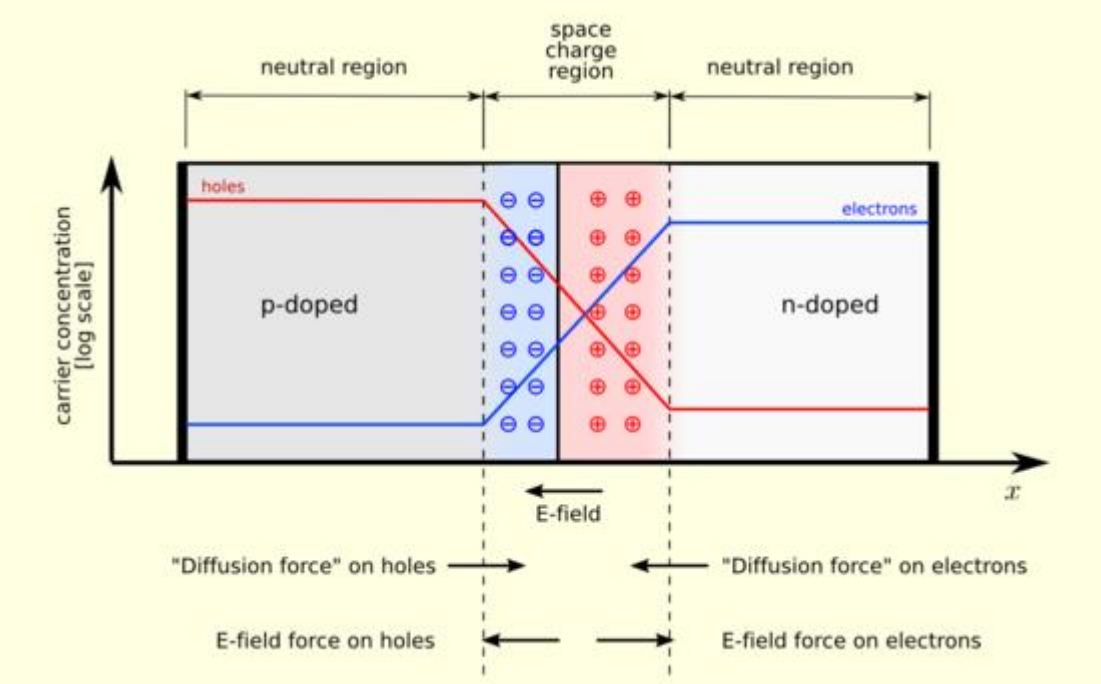
In a piece of sc, if one half is doped by p type impurity and the other half is doped by n type impurity, a PN junction is formed. The plane dividing the two halves or zones is called PN junction. As shown in the fig the n type material has high concentration of free electrons, while p type material has high concentration of holes. Therefore at the junction there is a tendency of

free electrons to diffuse over to the P side and the holes to the N side. This process is called

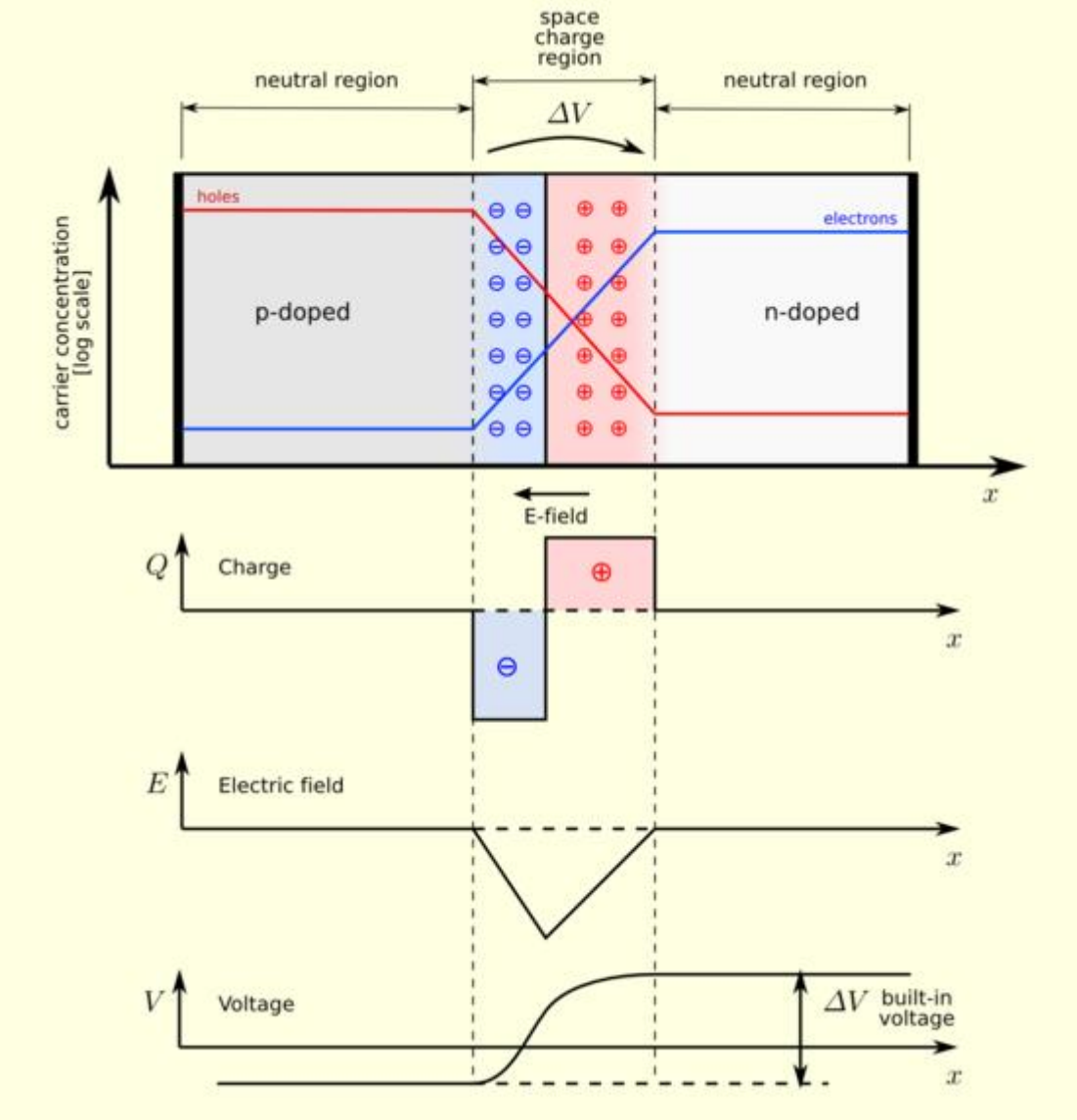


diffusion. As the free electrons move across the junction from N type to P type, the donor atoms become positively charged. Hence a positive charge is built on the N-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filing the holes. Therefore a negative charge is developed on the p side of the junction..This net negative charge on the p side prevents further diffusion of electrons into the p side. Similarly the net positive charge on the N side repels the hole crossing from p side to N side. Thus a barrier sis set up near the junction which prevents the further movement of charge carriers i.e. electrons and holes. As a consequence of induced electric field across the depletion layer, an electrostatic potential difference is established between P and N regions, which are called the potential barrier, junction barrier, diffusion potential or contact potential, Vo. The magnitude of the contact potential Vo varies with doping levels and temperature. Vo is 0.3V for Ge and 0.72 V for Si.

The electrostatic field across the junction caused by the positively charged N-Type region tends to drive the holes away from the junction and negatively charged p type regions tend to drive the electrons away from the junction. The majority holes diffusing out of the P region leave behind negatively charged acceptor atoms bound to the lattice, thus exposing a negatives pace charge in a previously neutral region. Similarly electrons diffusing from the N region expose positively ionized donor atoms and a double space charge builds up at the junction as shown in the fig. 1.7



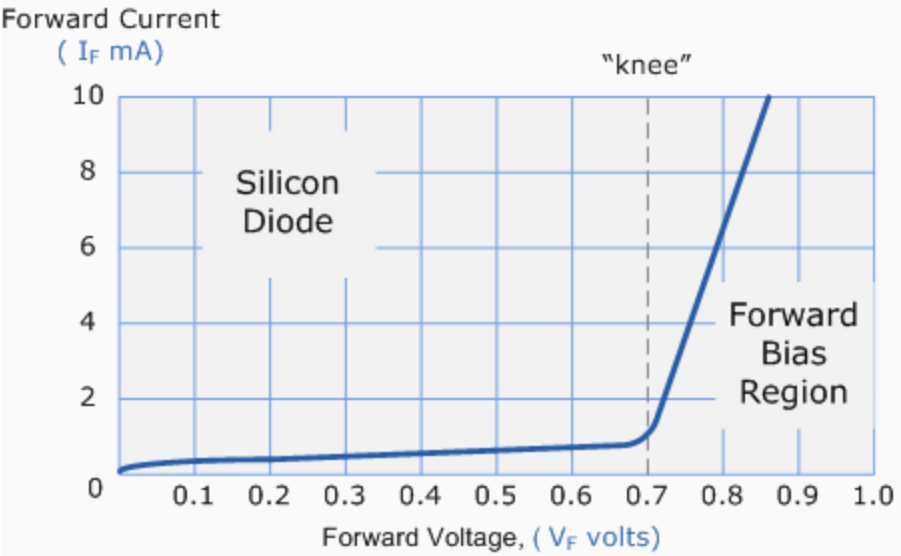
It is noticed that the space charge layers are of opposite sign to the majority carriers diffusing into them, which tends to reduce the diffusion rate. Thus the double space of the layer causes an electric field to be set up across the junction directed from N to P regions, which is in such a direction to inhibit the diffusion of majority electrons and holes as illustrated in fig 1.7. The shape of the charge density, ρ, depends upon how diode id doped. Thus the junction region is depleted of mobile charge carriers. Hence it is called depletion layer, space region, and transition region. The depletion region is of the order of 0.5µm thick. There are no mobile carriers in this narrow depletion region. Hence no current flows across the junction and the system is in equilibrium. To the left of this depletion layer, the carrier concentration is p= N_A and to its right it is n= N_D.



1.1.2 FORWARD BIASED JUNCTION DIODE

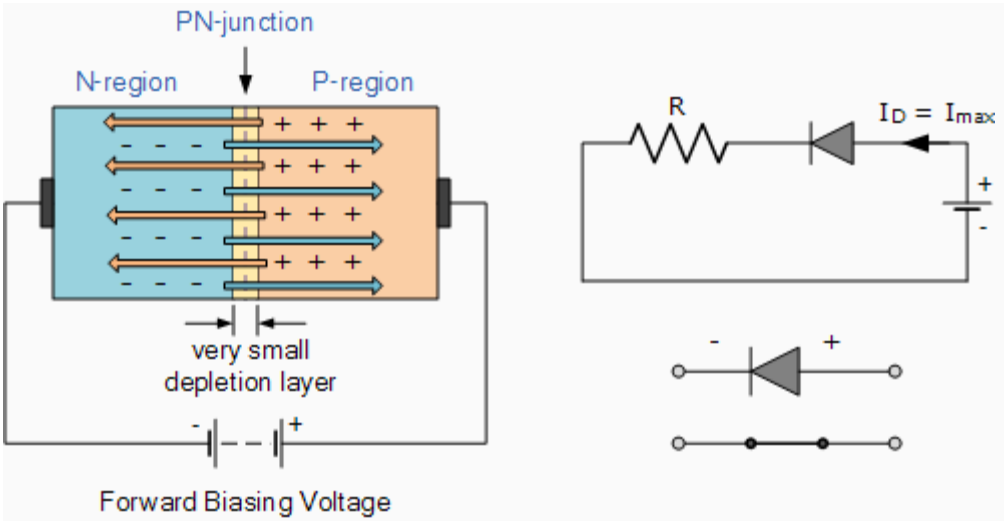
When a diode is connected in a **Forward Bias** condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow. This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.

Forward Characteristics Curve for a Junction Diode



The application of a forward biasing voltage on the junction diode results in the depletion layer becoming very thin and narrow which represents a low impedance path through the junction thereby allowing high currents to flow. The point at which this sudden increase in current takes place is represented on the static I-V characteristics curve above as the "knee" point.

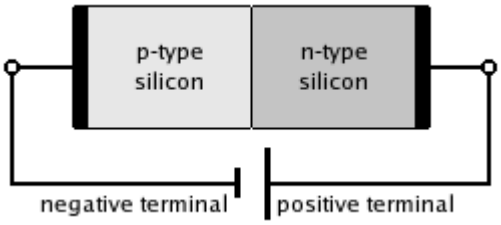
Forward Biased Junction Diode showing a Reduction in the Depletion Layer



This condition represents the low resistance path through the PN junction allowing very large currents to flow through the diode with only a small increase in bias voltage. The actual potential difference across the junction or diode is kept constant by the action of the depletion layer at approximately 0.3v for germanium and approximately 0.7v for silicon junction diodes. Since the diode can conduct "infinite" current above this knee point as it effectively becomes a

short circuit, therefore resistors are used in series with the diode to limit its current flow. Exceeding its maximum forward current specification causes the device to dissipate more power in the form of heat than it was designed for resulting in a very quick failure of the device.

1.1.2 PN JUNCTION UNDER REVERSE BIAS CONDITION:

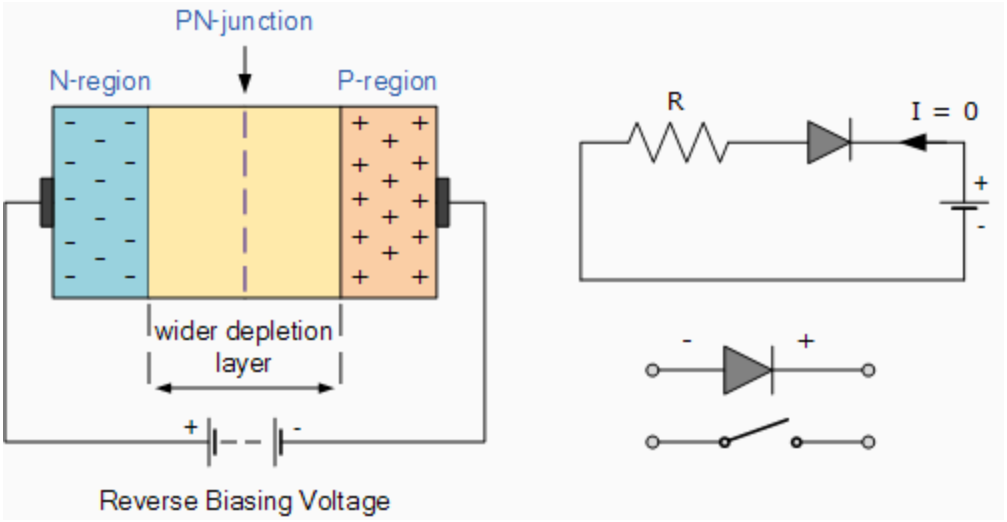


A silicon p– n junction in reverse bias.

Reverse Biased Junction Diode

When a diode is connected in a **Reverse Bias** condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode. The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

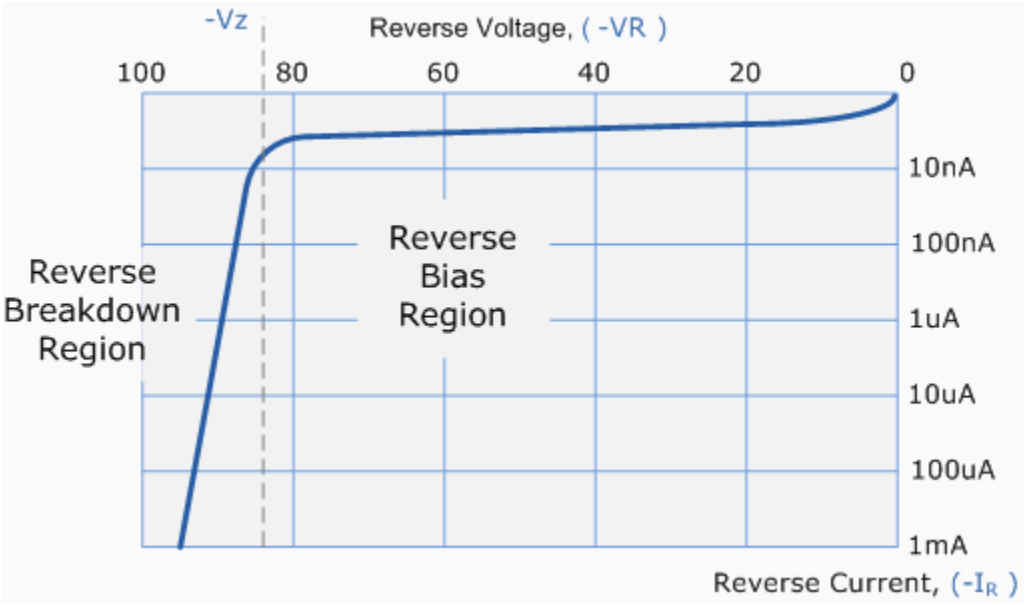
Reverse Biased Junction Diode showing an Increase in the Depletion Layer



This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small **leakage current** does flow through the junction

which can be measured in microamperes, (µA). One final point, if the reverse bias voltage Vr applied to the diode is increased to a sufficiently high enough value, it will cause the PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current, and this shown as a step downward slope in the reverse static characteristics curve below.

Reverse Characteristics Curve for a Junction Diode



Sometimes this avalanche effect has practical applications in voltage stabilising circuits where a series limiting resistor is used with the diode to limit this reverse breakdown current to a preset maximum value thereby producing a fixed voltage output across the diode. These types of diodes are commonly known as **Zener Diodes** and are discussed in a later tutorial.

1.2 VI CHARACTERISTICS AND THEIR TEMPERATURE DEPENDENCE:

Diode terminal characteristics equation for diode junction current:

$$I_D = I_0 (e^{\frac{v}{\eta v_T}} - 1)$$

Where VT = kT/q;

VD_ diode terminal voltage, Volts

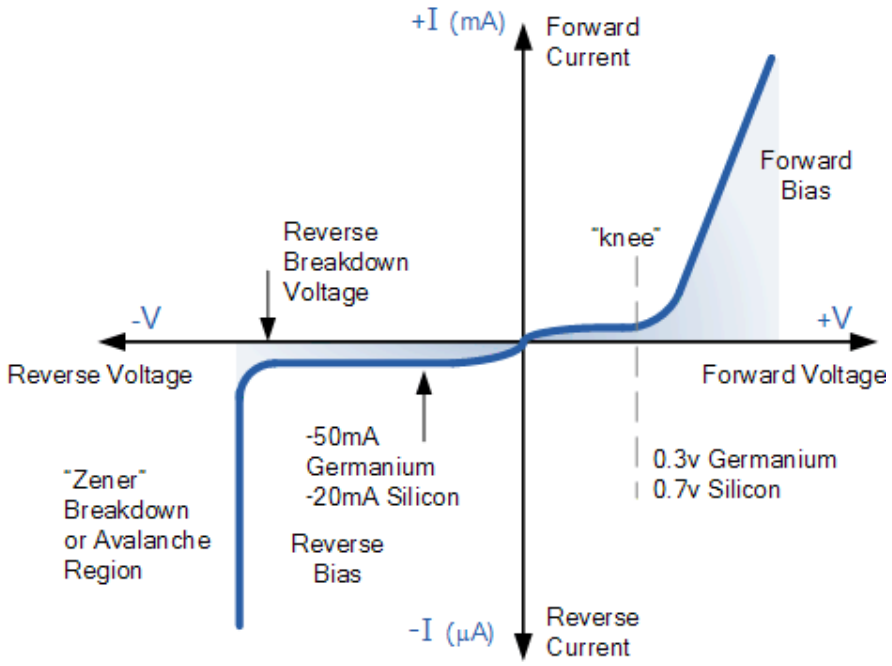
Io _ temperature-dependent saturation current, µA

T _ absolute temperature of p-n junction, K

k _ Boltzmann’ s constant 1.38x 10 -23J/K)

q _ electron charge 1.6x10-19 C

η = empirical constant, 1 for Ge and 2 for Si



Temperature Effects on Diode

Temperature can have a marked effect on the characteristics of a silicon semiconductor diode as shown in Fig. 1.24. It has been found experimentally that the reverse saturation current Io will just about double in magnitude for every 10°C increase in temperature.

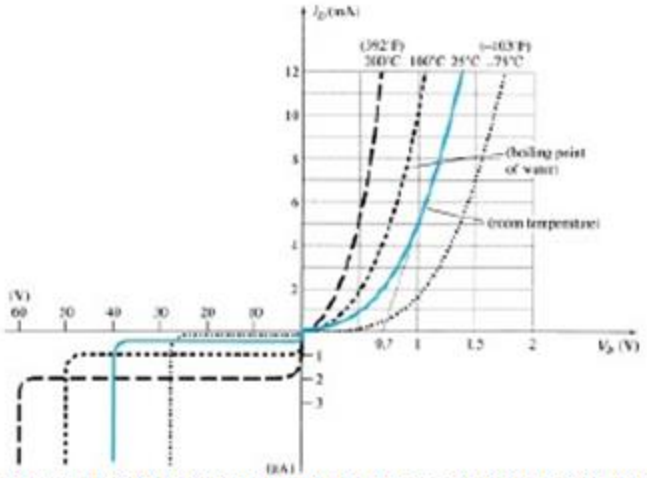


Figure 1.24 Variation in diode characteristics with temperature change.

It is not uncommon for a germanium diode with an Io in the order of 1 or 2 A at 25°C to have a leakage current of 100 A _ 0.1 mA at a temperature of 100°C. Typical values of Io for silicon are much lower than

that of germanium for similar power and current levels. The result is that even at high temperatures the levels of Io for silicon diodes do not reach the same high levels obtained.for germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design. Fundamentally, the open-circuit equivalent in the reverse bias region is better realized at any temperature with silicon than with germanium. The increasing levels of Io with temperature account for the lower levels of threshold voltage, as shown in Fig. 1.24. Simply increase the level of Io in and not rise in diode current. Of course, the level of TK also will be increase, but the increasing level of Io will overpower the smaller percent change in TK. As the temperature increases the forward characteristics are actually becoming more " ideal,"

1.3 IDEAL VERSUS PRACTICAL RESISTANCE LEVELS

DC or Static Resistance

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of VD and ID as shown in Fig. 1.25 and applying the following Equation:

$$R_D = \frac{V_D}{I_D}$$

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few mill amperes).

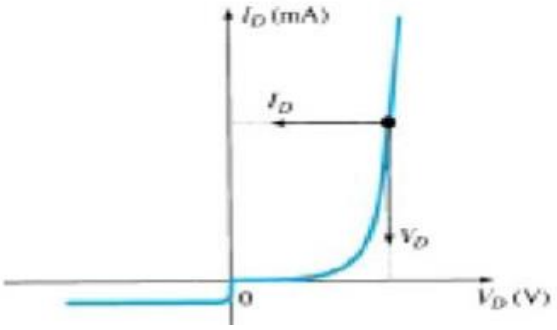


Figure 1.25 determining the dc resistance of a diode at a particular operating point.

AC or Dynamic Resistance

It is obvious from Eq. 1.5 that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.27. With no applied varying signal, the point of operation would be the Q-point appearing on Fig. 1.27 determined by the applied dc levels. The designation Q-point is derived from the word quiescent, which means " still or unvarying." A straight-line drawn tangent to the curve through the Q-point as shown in Fig. 1.28 will define a particular change in voltage and current that can be used to determine the ac or dynamic resistance for this region of the diode characteristics. In equation form,

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

where Δ signifies a finite change in the quantity.

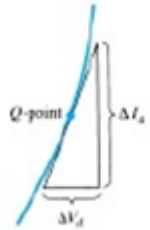


Figure 1.28 determining the ac resistance at a Q-point.

1.4 DIODE EQUIVALENT CIRCUITS

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device, system, or such in a particular operating region. In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behaviour of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

Piecewise-Linear Equivalent Circuit

One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig. 1.31. The resulting equivalent circuit is naturally called the piecewise-linear equivalent circuit. It should be obvious from Fig. 1.31 that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behaviour of the device. The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias

condition will result in the open- circuit state for the device. Since a silicon semiconductor, diode does not reach the conduction state until VD reaches 0.7 V with a forward bias (as shown in Fig. 1.31), a battery VT opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.32. The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established. When conduction is established, the resistance of the diode will be the specified value of rav.

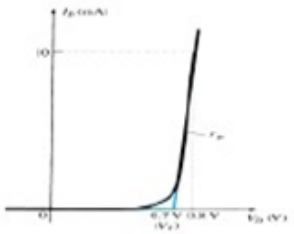


Figure 1.31 Defining the piecewise-linear equivalent circuit using straight-line segments to

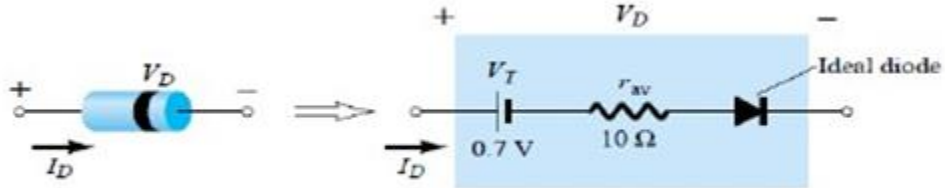


Figure 1.32 Components of the piecewise-linear equivalent circuit.

The approximate level of rav can usually be determined from a specified operating point on the specification sheet. For instance, for a silicon semiconductor diode, if IF _ 10 mA (a forward conduction current for the diode) at VD _ 0.8 V, we know for silicon that a shift of 0.7 V is required before the characteristics rise.

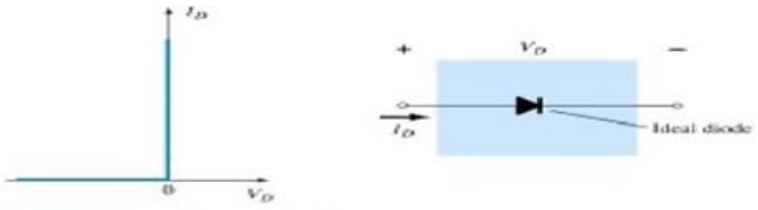
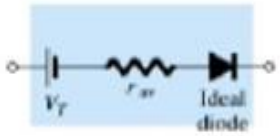
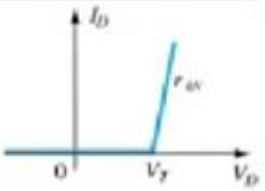
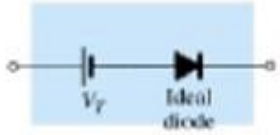
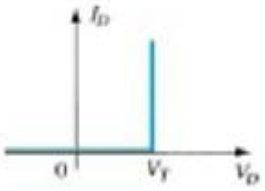
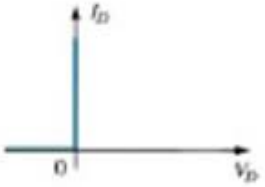


Figure 1.34 Ideal diode and its characteristics.

TABLE 1.3 Diode Equivalent Circuits (Models)

Type	Conditions	Model	Characteristics
Piecewise-linear model			
Simplified model	$R_{network} \gg r_{av}$		
Ideal device	$R_{network} \gg r_{av}$ $E_{network} \gg V_T$		

1.5 TRANSITION AND DIFFUSION CAPACITANCE

Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects that can be ignored at lower frequencies because the reactance XC=1/2πfC is very large (open-circuit equivalent). This, however, cannot be ignored at very high frequencies. XC will become sufficiently small due to the high value of f to introduce a low-reactance " shorting" path. In the p-n semiconductor diode, there are two capacitive effects to be considered. In the reverse-bias region we have the transition- or depletion region capacitance (CT), while in the forward-bias region we have the diffusion (CD) or storage capacitance. Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by C=€A/d, where € is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d. In the reverse-, bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (d) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease. The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. Although the effect described above will also be present in the forward-bias region, it is over shadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions

Fig 1.7d. VI characteristics of ideal diode

just outside the depletion region. The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in Fig. 1.38. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.

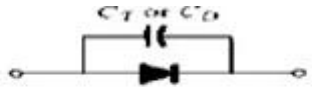


Figure 1.38 Including the effect of the transition or diffusion capacitance on the semiconductor diode.

Diode capacitances: The diode exhibits two types of capacitances transition capacitance and diffusion capacitance.

. Transition capacitance: The capacitance which appears between positive ion layer in n-region and negative ion layer in p-region.

· Diffusion capacitance: This capacitance originates due to diffusion of charge carriers in the opposite regions.

The transition capacitance is very small as compared to the diffusion capacitance.

In reverse bias transition, the capacitance is the dominant and is given by:

$$C_T = \epsilon A/W$$

where C_T - transition capacitance

A - diode cross sectional area

W - depletion region width

In forward bias, the diffusion capacitance is the dominant and is given by:

$$C_D = dQ/dV = \tau^* dI/dV = \tau^* g = \tau/r \text{ (general)}$$

where C_D - diffusion capacitance

dQ - change in charge stored in depletion region

V - change in applied voltage

τ - time interval for change in voltage

g - diode conductance

r - diode resistance

The diffusion capacitance at low frequencies is given by the formula:

$C_D = \tau^* g/2$ (low frequency)

The diffusion capacitance at high frequencies is inversely proportional to the frequency and is given by the formula:

$C_D = g(\tau/2\omega)^{1/2}$

Note: The variation of diffusion capacitance with applied voltage is used in the design of varactor.

1.6 BREAK DOWN MECHANISMS

When an ordinary **P-N junction diode** is reverse biased, normally only very small reverse saturation current flows. This current is due to movement of minority carriers. It is almost independent of the voltage applied. However, if the reverse bias is increased, a point is reached when the junction breaks down and the reverse current increases abruptly. This current could be large enough to destroy the junction. If the reverse current is limited by means of a suitable series resistor, the power dissipation at the junction will not be excessive, and the device may be operated continuously in its breakdown region to its normal (reverse saturation) level. It is found that for a suitably designed diode, the breakdown voltage is very stable over a wide range of reverse currents. This quality gives the *breakdown **diode*** many useful applications as a *voltage reference source.*

The critical value of the voltage, at which the breakdown of a P-N junction diode occurs is called the *breakdown voltage.* The breakdown voltage depends on the width of the depletion region, which, in turn, depends on the doping level. The junction offers almost zero resistance at the breakdown point.

There are two mechanisms by which breakdown can occur at a reverse biased P-N junction :

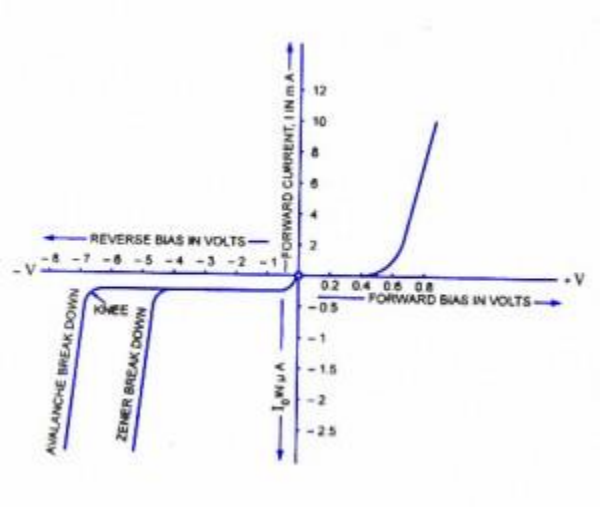
1. ***avalanche breakdown*** **and**
2. ***Zener breakdown.***

Avalanche breakdown **and**

The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5 V or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material. As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown. *The breakdown region is the knee of the characteristic curve. Now the current is not controlled by the junction voltage but rather by the external circuit.*

Zener breakdown

Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3 x 10^7 V/m.



Either of the two (Zener breakdown or avalanche breakdown) may occur independently, or both of these may occur simultaneously. Diode junctions that breakdown below 5 V are caused by Zener effect. Junctions that experience breakdown above 5 V are caused by avalanche effect. Junctions that breakdown around 5 V are usually caused by combination of two effects. The Zener breakdown occurs in heavily doped junctions (P-type semiconductor moderately doped and N-type heavily doped), which produce narrow depletion layers. The avalanche breakdown occurs in lightly doped junctions, which produce wide depletion layers. With the increase in junction temperature Zener breakdown voltage is reduced while the avalanche breakdown voltage increases. The Zener diodes have a negative temperature coefficient while avalanche diodes have a positive temperature coefficient. Diodes that have breakdown voltages around 5 V have zero temperature coefficient. The breakdown phenomenon is reversible and harmless so long as the safe operating temperature is maintained.

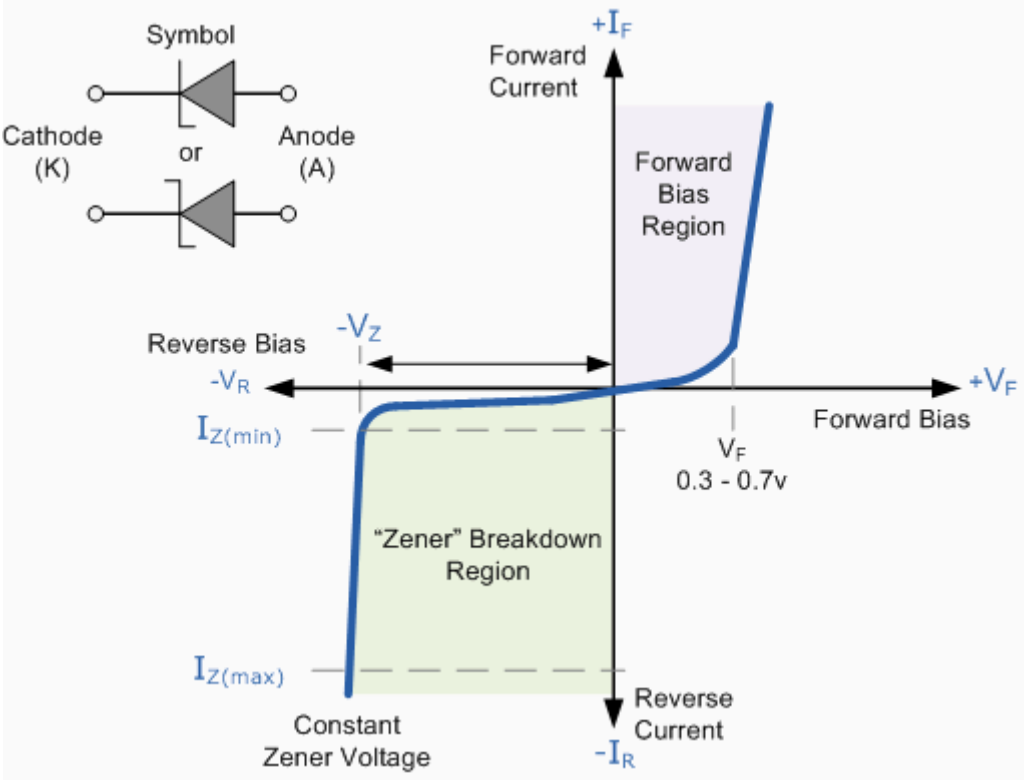
1.7 ZENER DIODES

The **Zener diode** is like a general-purpose signal diode consisting of a silicon PN junction. When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but as soon as a reverse voltage applied across the zener diode exceeds the rated voltage of the device, the diodes breakdown voltage V_B is reached at which point a process called *Avalanche Breakdown* occurs in the semiconductor depletion layer and a current starts to flow through the diode to limit this increase in voltage.

The current now flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor) and once achived this reverse saturation current remains fairly constant over a wide range of applied voltages. This breakdown voltage point, V_B is called the "zener voltage" for zener diodes and can range from less than one volt to hundreds of volts.

The point at which the zener voltage triggers the current to flow through the diode can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes semiconductor construction giving the diode a specific *zener breakdown voltage*, (V_Z) for example, 4.3V or 7.5V. This zener breakdown voltage on the I-V curve is almost a vertical straight line.

Zener Diode I-V Characteristics



The **Zener Diode** is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply. From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current $I_{Z(min)}$ and the maximum current rating $I_{Z(max)}$.

This ability to control itself can be used to great effect to regulate or stabilise a voltage source against supply or load variations. The fact that the voltage across the diode in the breakdown region is almost constant turns out to be an important application of the zener diode as a voltage regulator. The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum $I_{Z(min)}$ value in the reverse breakdown region.

UNIT-II
SPECIAL DIODES AND RECTIFIERS

Content:

Special Diodes: Zener Diode – V-I characteristics, Applications, Breakdown Mechanisms-Zener Breakdown and Avalanche Breakdown, Construction, Operation, Characteristics and applications of LED, LCD, Photodiode, Varactor Diode and Tunnel diode.

Rectifiers: Basic Rectifier setup, Half wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Inductive and Capacitive Filters, L-Section(CLC filter) and P-section, Rectifier parameters with and without filters.

SPECIAL DIODES

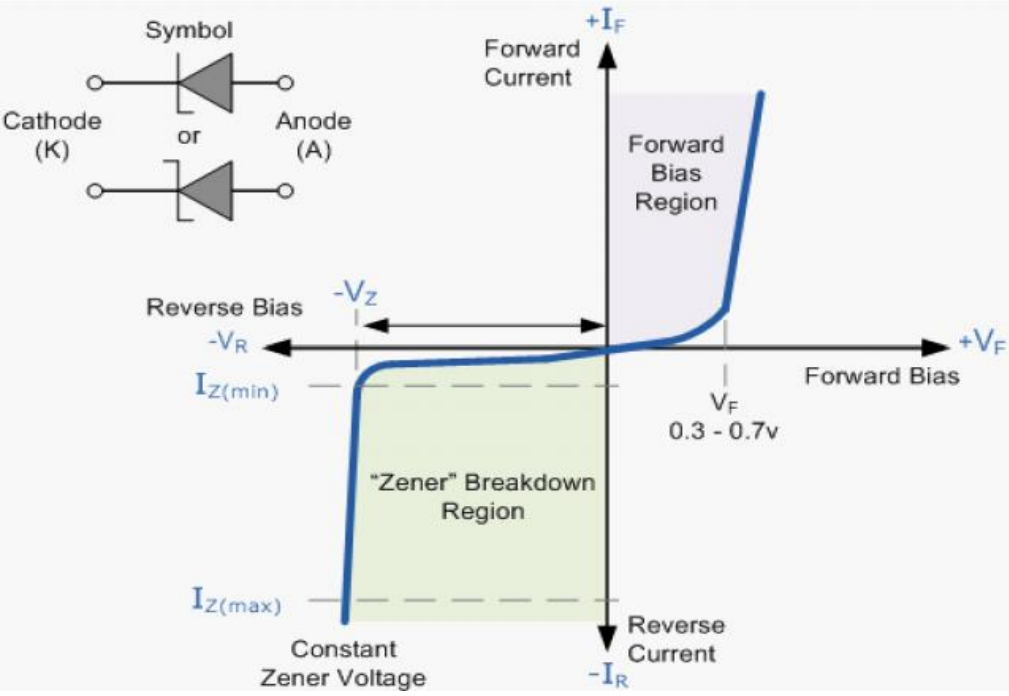
Zener Diode:

A Zener diode is a heavily doped semiconductor device that is designed to operate in the reverse direction. The Zener diode is like a general-purpose signal diode consisting of a silicon PN junction. When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but as soon as a reverse voltage applied across the zener diode exceeds the rated voltage of the device, the diodes breakdown voltage VB is reached at which point a process called Avalanche Breakdown occurs in the semiconductor depletion layer and a current starts to flow through the diode to limit this increase in voltage.

The current now flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor) and once achieved this reverse saturation current remains fairly constant over a wide range of applied voltages. This breakdown voltage point, VB is called the "zener voltage" for zener diodes and can range from less than one volt to hundreds of volts.

The point at which the zener voltage triggers the current to flow through the diode can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes semiconductor construction giving the diode a specific zener breakdown voltage, (Vz) for example, 4.3V or 7.5V. This zener breakdown voltage on the I-V curve is almost a vertical straight line.

Zener Diode I-V Characteristics



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This ability to control itself can be used to great effect to regulate or stabilize a voltage source against supply or load variations. The fact that the voltage across the diode in the breakdown region is almost constant turns out to be an important application of the zener diode as a voltage regulator. The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum IZ (min)value in the reverse breakdown region.

Avalanche Breakdown in Zener Diode

Avalanche breakdown occurs both in normal diode and Zener Diode at high reverse voltage. When a high value of reverse voltage is applied to the PN junction, the free electrons gain sufficient energy and accelerate at high velocities. These free electrons moving at high velocity collides other atoms and knocks off more electrons. Due to this continuous collision, a large number of free electrons are generated as a result of electric current in the diode rapidly increases. This sudden increase in electric current may permanently destroy the normal diode, however, a Zener diode is designed to operate under avalanche breakdown and can sustain the sudden spike of current. Avalanche breakdown occurs in Zener diodes with Zener voltage (Vz) greater than 6V.

Zener Breakdown in Zener Diode

When the applied reverse bias voltage reaches closer to the Zener voltage, the electric field in the depletion region gets strong enough to pull electrons from their valence band. The valence electrons that gain sufficient energy from the strong electric field of the depletion region break free from the parent atom. At the Zener breakdown region, a small increase in the voltage results in the rapid increase of the electric current.

Applications of Zener Diode

- As a voltage regulator.
- Protects from over voltage.
- Used in clipping circuits.
- Used to shift voltage.

TUNNELDIODE

A tunnel diode or Esaki diode is a type of semiconductor diode which is capable of very fast operation, well into the microwave frequency region, by using quantum mechanical effects.

It was invented in August 1957 by Leo Esaki when he was with Tokyo Tsushin Kogyo, now known as Sony. In 1973 he received the Nobel Prize in Physics, jointly with Brian Josephson, for discovering the electron tunneling effect used in these diodes. Robert Noyce independently came up with the idea of a tunnel diode while working for William Shockley but was discouraged from pursuing it.

Fig: Tunnel diode schematic symbol

These diodes have a heavily doped p–n junction only some 10 nm (100 Å) wide. The heavy doping results in a broken bandgap, where conduction band electron states on the n-side are more or less aligned with valence band hole states on the p-side.

Tunnel diodes were manufactured by Sony for the first time in 1957 followed by General Electric and other companies from about 1960 and are still made in low volume today. Tunnel diodes are usually made from germanium but can also be made in gallium arsenide and silicon materials. They can be used as oscillators, amplifiers, frequency converters and detectors.

Tunnelling Phenomenon

In a conventional semiconductor diode, conduction takes place while the p–n junction is forward biased and blocks current flow when the junction is reverse biased. This occurs up to a point known as the “reverse breakdown voltage” when conduction begins (often accompanied by destruction of the device). In the tunnel diode, the dopant concentration in the p and n layers are increased to the

point 53 where the reverse breakdown voltage becomes zero and the diode conducts in the reverse direction. However, when forward biased, an odd effect occurs called "quantum mechanical tunnelling" which gives rise to a region where an increase in forward voltage is accompanied by a decrease in forward current. This negative resistance region can be exploited in a solid-state version of the dynatron oscillator which normally uses a tetrode thermionic valve (or tube).

Forward bias operation

Under normal forward bias operation, as voltage begins to increase, electrons at first tunnel through the very narrow p–n junction barrier because filled electron states in the conduction band on the n-side become aligned with empty valence band hole states on the p-side of the p-n junction. As voltage increases further these states become more misaligned and the current drops – this is called negative resistance because current decreases with increasing voltage. As voltage increases yet further, the diode begins to operate as a normal diode, where electrons travel by conduction across the p–n junction, and no longer by tunneling through the p–n junction barrier. Thus, the most important operating region for a tunnel diode is the negative resistance region.

Reverse bias operation

When used in the reverse direction they are called back diodes and can act as fast rectifiers with zero offset voltage and extreme linearity for power signals (they have an accurate square law characteristic in the reverse direction). Under reverse bias filled states on the p-side become increasingly aligned with empty states on the nside and electrons now tunnel through the pn junction barrier in reverse direction – this is the Zener effect that also occurs in zener diodes.

Advantages of tunnel diodes:

- Environmental immunity i.e peak point is not a function of temperature.
- low cost.
- low noise.
- low power consumption.
- High speed i.e., tunneling takes place very fast at the speed of light in the order of
- nanoseconds
- simplicity i.e., a tunnel diode can be used along with a D.C supply and a few passive.
- elements to obtain various application circuits.

Applications for tunnel diodes:

- local oscillators for UHF television tuners

- Trigger circuits in oscilloscopes
- High speed counter circuits and very fast-rise time pulse generator circuits
- The tunnel diode can also be used as low-noise microwave amplifier.

Varactor Diode:

Varactor diode is a special type of diode which uses transition capacitance property i.e voltage variable capacitance .These are also called as varicap,VVC(voltage variable capacitance) or tuning diodes. The varactor diode symbol is shown below with a diagram representation.

Fig: symbol of varactor diode

When a reverse voltage is applied to a PN junction, the holes in the p-region are attracted to the anode terminal and electrons in the n-region are attracted to the cathode terminal creating a region where there is little current. This region, the depletion region, is essentially devoid of carriers and behaves as the dielectric of a capacitor.

The depletion region increases as reverse voltage across it increases; and since capacitance varies inversely as dielectric thickness, the junction capacitance will decrease as the voltage across the PN junction increases. So, by varying the reverse voltage across a PN junction the junction capacitance can be varied.

Applications:

- Tuned circuits.
- FM modulators
- Automatic frequency control devices
- Adjustable bandpass filters
- Parametric amplifiers
- Television receivers.

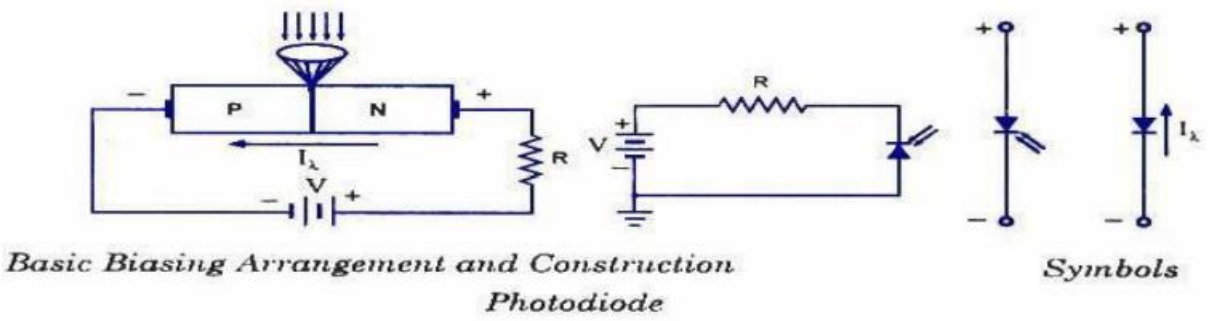
Photodiode:

The photo diode is a semiconductor p-n junction device whose region of operation is limited to the reverse biased region. The figure below shows the symbol of photodiode.

Fig: Symbol for photodiode.

Principle of operation:

A photodiode is a type of photo detector capable of converting light into either current or voltage, depending upon the mode of operation. The common, traditional solar cell used to generate electric solar power is a large area photodiode. A photodiode is designed to operate in reverse bias. The deletion region width is large. Under normal conditions it carries small reverse current due to minority charge carriers. When light is incident through glass window on the p-n junction, photons in the light bombard the p-n junction and some energy s imparted to the valence electrons. So valence electrons break covalent bonds and become free electrons. Thus more electron-hole pairs are generated. Thus total number of minority charge carriers increases and hence reverse current increases. This is the basic principle of operation of photodiode.



Characteristics of photodiode:

When the P-N junction is reverse-biased, a reverse saturation current flows due to thermally generated holes and electrons being swept across the junction as the minority carriers. With the increase in temperature of the junction more and more hole-electron pairs are created and so the reverse saturation current I0 increases. The same effect can be had by illuminating the junction. When light energy bombards a P-N junction, it dislodges valence electrons. The more light striking the junction the larger the reverse current in a diode. It is due to generation of more and more charge carriers with the increase in level of illumination. This is clearly shown in ‘figure for different intensity levels. The dark current is the current that exists when no light is incident. It

is to be noted here that current becomes zero only with a positive applied bias equal to VQ. The almost equal spacing between the curves for the same increment in luminous flux reveals that the reverse saturation current I0increases linearly with the luminous flux as shown in figure. Increase in reverse voltage does not increase the reverse current significantly, because all available charge carriers are already being swept across the junction. For reducing the reverse saturation current I0 to zero, it is necessary to forward bias the junction by an amount equal to barrier potential. Thus, the photodiode can be used as a photoconductive device.

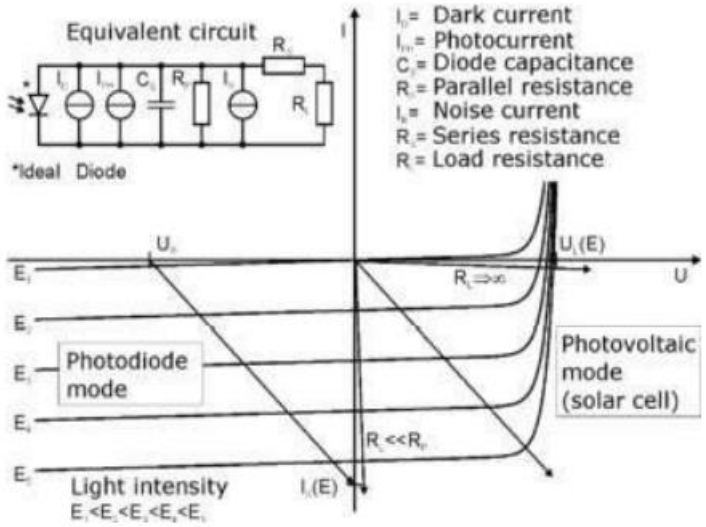


Fig: characteristics of photodiode

On removal of reverse bias applied across the photodiode, minority charge carriers continue to be swept across the junction while the diode is illuminated. This has the effect of increasing the concentration of holes in the P-side and that of electrons in the N-side But the barrier potential is negative on the P-side and positive on the N-side, and was created by holes flowing from P to Nside and electrons from N to P-side during fabrication of junction. Thus the flow of minority carriers tends to reduce the barrier potential.

When an external circuit is connected across the diode terminals, the minority carrier; return to the original side via the external circuit. The electrons which crossed the junction from P to Nside now flow out through the N-terminal and into the P-terminal This means that the device is behaving as a voltage cell with the N-side being the negative terminal and the P-side the positive terminal. Thus, the photodiode is & photovoltaic device as well as photoconductive device.

Advantages:

The advantages of photodiode are:

1.It can be used as variable resistance device.

2.Highly sensitive to the light.

3.The speed of operation is very high.

Disadvantages:

1.Temperature dependent dark current.
2.poor temperature stability.
3.Current needs amplification for driving other circuits.

Applications:

1.Alarm system.
2.counting system.

LCD (Liquid Crystal Display):

A liquid crystal display or LCD draws its definition from its name itself. It is a combination of two states of matter, the solid and the liquid. LCD uses a liquid crystal to produce a visible image. Liquid crystal displays are super-thin technology. We always use devices made up of Liquid Crystal Displays (LCDs) like computers, digital watches and also DVD and CD players. They have become very common and have taken a giant leap in the screen industry by clearly replacing the use of Cathode Ray Tubes (CRT). CRT draws more power than LCD and are also bigger and heavier. All of us have seen an LCD, but only few knows how exactly they work.

Working of LCD: The main principle behind liquid crystal molecules is that when an electric current is applied to them, they tend to untwist. This causes a change in the light angle passing through them. This causes a change in the angle of the top polarizing filter with respect to it. So little light is allowed to pass through that particular area of LCD. Thus, that area becomes darker comparing to others. For making an LCD screen, a reflective mirror has to be setup in the back. An electrode plane made of indium-tin oxide is kept on top and a glass with a polarizing film is also added on the bottom side. The entire area of the LCD has to be covered by a common electrode and above it should be the liquid crystal substance. Next comes another piece of glass with an electrode in the shape of the rectangle on the bottom and, on top, another polarizing film. It must be noted that both of them are kept at right angles. When there is no current, the light passes through the front of the LCD it will be reflected by the mirror and bounced back. As the electrode is connected to a temporary battery the current from it will cause the liquid crystals between the common-plane electrode and the electrode shaped like a rectangle to untwist. Thus, the light is blocked from passing through. Thus, that particular rectangular area appears blank.

Characteristics of LCD:

1. The resolution of LCD can be very high, and the PPI (pixels per inch) of general mobile phones can reach more than 300.

2. LCD grayscale more, can display a wider range of colors.

3. TFT LCD high display quality:
because the LCD screen every point after receiving the signal has been maintained the color and brightness, constant luminescence, and not like the cathode ray tube display (CRT) need to constantly refresh bright spots. Therefore, the LCD picture quality is high and absolutely does not blink, reducing eye fatigue to a minimum.

4. TFT LCD screen no electromagnetic radiation:
Traditional screen display material is a phosphor, by electron beam phosphors impact, according to the electron beam in the hit for a moment on the fluorescent powder can produce strong electromagnetic radiation, although there are many display products is more effective in the treatment of the radiation on the processing, as much as possible to minimize radiation, but it is difficult to eliminate. Liquid crystal displays (LCDs), by contrast, have an innate advantage in preventing radiation because they do not exist. In the prevention of electromagnetic wave, the LCD screen also has its own unique advantages, it has adopted strict sealing technology will come from the power circuit of the closed a small number of electromagnetic waves in the screen, and the need for ordinary display in order to send out the quantity of heat must let the internal circuit is exposed to air as much as possible so that the internal circuit of the electromagnetic wave is a lot to "leak".

Applications:

- Liquid crystal thermometer
- Optical imaging
- The liquid crystal display technology is also applicable in the visualization of the radio frequency waves in the waveguide.
- Used in the medical applications.

LED (Light Emitting Diode):

Light Emitting Diodes or LED´s, are among the most widely used of all the different types of semiconductor diodes available today and are commonly used in TV’s and colour displays. They are the most visible type of diode, that emit a fairly narrow bandwidth of either visible light at different coloured wavelengths, invisible infra-red light for remote controls or laser type light when a forward current is passed through them.

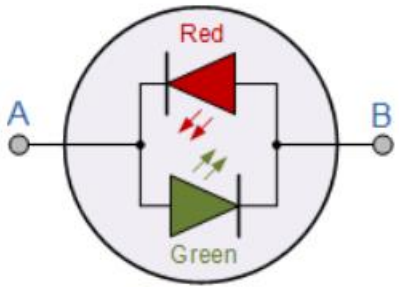


Fig: The Light Emitting Diode

The “Light Emitting Diode” or as it is more commonly called, is basically just a specialised type of diode as they have very similar electrical characteristics to a PN junction diode. This means that an LED will pass current in its forward direction but block the flow of current in the reverse direction.
Related Products: LEDs and LED Lighting | Optical Lenses

Light emitting diodes are made from a very thin layer of fairly heavily doped semiconductor material and depending on the semiconductor material used and the amount of doping, when forward biased an LED will emit a coloured light at a particular spectral wavelength. When the diode is forward biased, electrons from the semiconductors conduction band recombine with holes from the valence band releasing sufficient energy to produce photons which emit a monochromatic (single colour) of light. Because of this thin layer a reasonable number of these photons can leave the junction and radiate away producing a coloured light output.

Fig: LED Construction

Then we can say that when operated in a forward biased direction Light Emitting Diodes are semiconductor devices that convert electrical energy into light energy. The construction of a Light Emitting Diode is very different from that of a normal signal diode. The PN junction of an LED is surrounded by a transparent, hard plastic epoxy resin hemispherical shaped shell or body which

protects the LED from both vibration and shock. Surprisingly, an LED junction does not actually emit that much light, so the epoxy resin body is constructed in such a way that the photons of light emitted by the junction are reflected away from the surrounding substrate base to which the diode is attached and are focused upwards through the domed top of the LED, which itself acts like a lens concentrating the amount of light. Therefore, the emitted light appears to be brightest at the top of the LED.

However, not all LEDs are made with a hemispherical shaped dome for their epoxy shell. Some indication LEDs have a rectangular or cylindrical shaped construction that has a flat surface on top or their body is shaped into a bar or arrow. Generally, all LED's are manufactured with two legs protruding from the bottom of the body.

Also, nearly all modern light emitting diodes have their cathode, (–) terminal identified by either a notch or flat spot on the body or by the cathode lead being shorter than the other as the anode (+) lead is longer than the cathode (k). Unlike normal incandescent lamps and bulbs which generate large amounts of heat when illuminated, the light emitting diode produces a "cold" generation of light which leads to high efficiencies than the normal "light bulb" because most of the generated energy radiates away within the visible spectrum. Because LEDs are solid-state devices, they can be extremely small and durable and provide much longer lamp life than normal light sources.

Characteristics of LED:

LEDs are solid-state devices. The advantages are:

1) Light Generated by LED is Directional

- LED is all forward directional lighting, not Omni as conventional light bulb.
- In general, beam angel is around 140 degree.
- Utilize this directional characteristics and employee optical lens can achieve different light patterns.

2) LED can Generate Different Light Color

- Wavelength determinate light color output: red, green, blue, yellow, or purple.
- RGB light mix or different phosphor mix will create white light.

3) Temperature will Affect LED Efficacy

- LED itself will generate heat, which will affect efficacy as well as LED life.
- In general, 10 Degree increase will reduce 5 – 7% lumen output

- Maintain P-N Junction temperature under 75 degree will enable LED last for over 50,000 hours.

4) Low Energy Consumption

- 100 lm/W is commercialized, while over 200lm/W is achieved in lab.
- I Less than 1/5 to 1/10 power consumption of conventional lighting is achieving or 80% to 90% of energy will be saved.

5) Long Life

- No fragile parts, as conventional light bulb, to be broken.
- Light will decay lumen output, but rarely burn out or dead.
- A well-designed luminaire expects over 70% lumen maintenance at 50,000 hours usage.

RECTIFIER

A rectifier is an electrical component that converts alternating current (AC) to direct current (DC). A rectifier is analogous to a one-way valve that allows an electrical current to flow in only one direction. The process of converting AC current to DC current is known as rectification. A rectifier can take several physical forms such as solid-state diodes, vacuum tube diodes, mercury-arc valves, silicon-controlled rectifiers, and various other silicon-based semiconductor switches.

Types of Rectifier:

1) Half wave Rectifier.
2) Full wave Rectifier.
3) Bridge Rectifier.

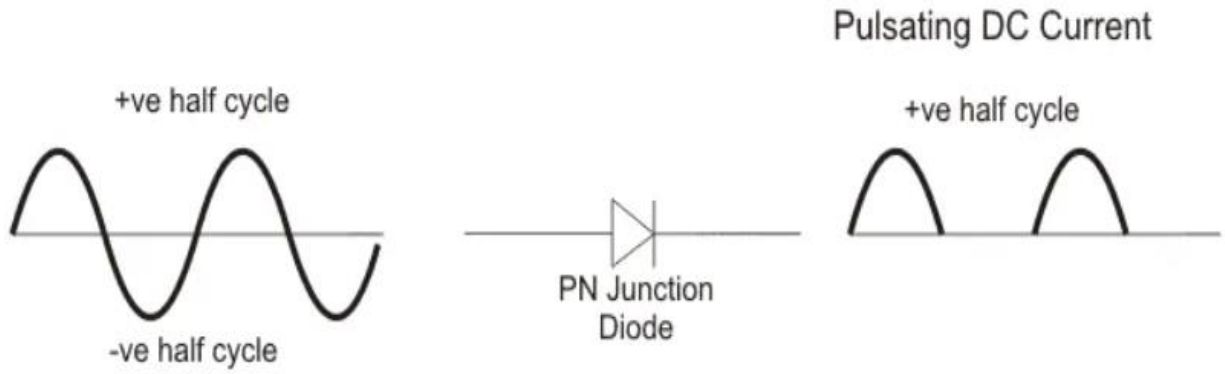
Half Wave Rectifier:

A half wave rectifier is defined as a type of rectifier that only allows one half-cycle of an AC voltage waveform to pass, blocking the other half-cycle. Half-wave rectifiers are used to convert AC voltage to DC voltage, and only require a single diode to construct.

A half wave rectifier is the simplest form of rectifier available. We will look at a complete half wave rectifier circuit later – but let's first understand exactly what this type of rectifier is doing.

The diagram below illustrates the basic principle of a half-wave rectifier. When a standard AC

waveform is passed through a half-wave rectifier, only half of the AC waveform remains. Half-wave rectifiers only allow one half-cycle (positive or negative half-cycle) of the AC voltage through and will block the other half-cycle on the DC side, as seen below.



Only one diode is required to construct a half-wave rectifier. In essence, this is all that the half-wave rectifier is doing.

Since DC systems are designed to have current flowing in a single direction (and constant voltage – which we'll describe later), putting an AC waveform with positive and negative cycles through a DC device can have destructive (and dangerous) consequences. So we use half-wave rectifiers to convert the AC input power into DC output power.

But the diode is only part of it – a complete half-wave rectifier circuit consists of 3 main parts:

1) A Transformer.
2) A Resistive Load.
3) A Diode

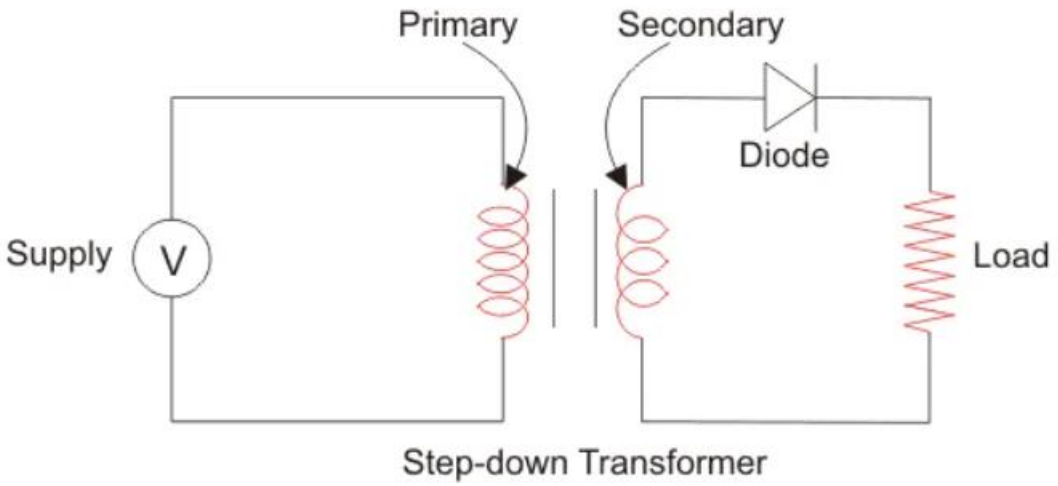
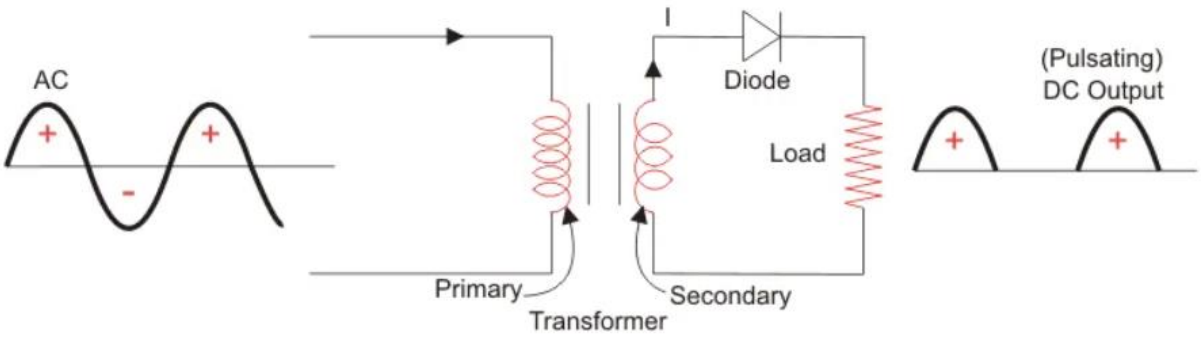


Fig: Half wave rectifier

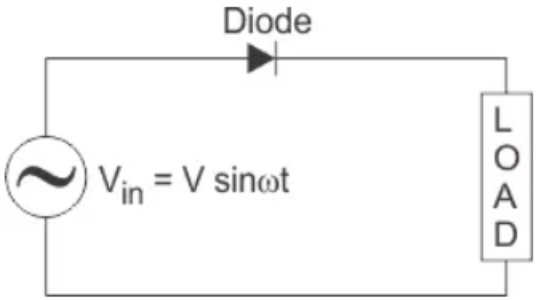
First, a high AC voltage is applied to the to the primary side of the step-down transformer and we will get a low voltage at the secondary winding which will be applied to the diode.

During the positive half cycle of the AC voltage, the diode will be forward biased and the current flows through the diode.

During the negative half cycle of the AC voltage, the diode will be reverse biased and the flow of current will be blocked. The final output voltage waveform on the secondary side (DC) is shown in figure.



We will focus on the secondary side of the circuit. If we replace the secondary transformer coils with a source voltage, we can simplify the circuit diagram of the half-wave rectifier as:



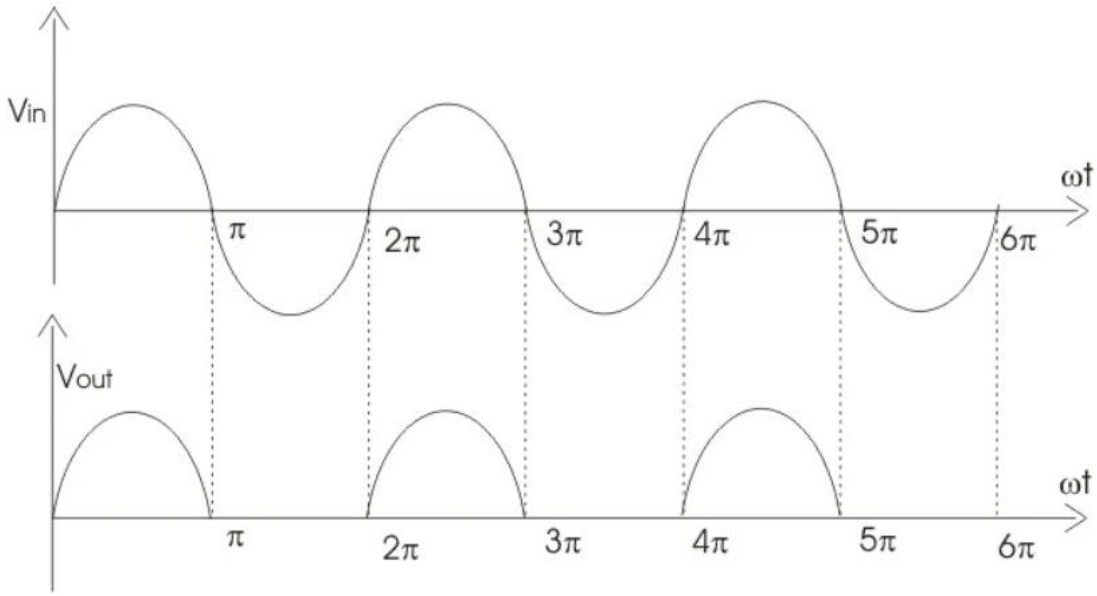
For the positive half cycle of the AC source voltage, the diode is forward biased, and is hence allowing current to pass through. So we have a closed circuit.

But for the negative half cycle of the AC source voltage, the diode is now in reverse bias mode, no current is able to pass through it. As such, we now have an open circuit. Since current can not flow through to the load during this time, the output voltage is equal to zero.

This all happens very quickly – since an AC waveform will oscillate between positive and negative many times each second (depending on the frequency).

Here's what the half wave rectifier waveform looks like on the input side (Vin), and what it looks like on the output side (Vout) after rectification (i.e. conversion from AC to DC):

The graph below shows a positive half wave rectifier. This is a half-wave rectifier which only allows the positive half-cycles through the diode, and blocks the negative half-cycle.



Calculations:

Without Filter:

$V_{rms} = V_m / 2$

$$V_{dc} = \frac{V_m}{\pi}$$

Ripple factor (Theoretical) $$= \sqrt{(\frac{V_{rms}}{V_{dc}})^2 - 1} = 1.21$$

Ripple Factor(practical) $\gamma = \frac{V_{ac}}{V_{dc}}$ where $V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$

With Filter:

Ripple Factor (Theoretical) $$r = \frac{1}{2\sqrt{3}fCR}$$

Where f = 50Hz, R = 1KΩ, C = 1000μF

$$V_{ac} = \frac{V_{r(p-p)}}{2\sqrt{3}}$$

$$V_{dc} = V_m - \frac{V_{r(p-p)}}{2}$$

Ripple Factor(practical) = $$\gamma = \frac{V_{ac}}{V_{dc}}$$

Percentage Regulation $$= \frac{V_{NL} - V_{FL}}{V_{FL}} * 100$$ %

V_{NL} = DC voltage at the load without connecting the load (Minimum current).

V_{FL} = DC voltage at the load with load connected.

Efficiency = $\eta = \frac{P_{DC}}{P_{AC}}$

$P_{AC} = V_{2rms} / R_L$

$P_{DC} = V_{dc} / R_L$

Applications of Half Wave Rectifier

Half wave rectifiers are not as commonly used as full-wave rectifiers. Despite this, they still have some uses:

- For rectification applications
- For signal demodulation applications
- For signal peak applications

Advantages of Half Wave Rectifier

The main advantage of half-wave rectifiers is in their simplicity. As they don't require as many components, they are simpler and cheaper to setup and construct.
As such, the main advantages of half-wave rectifiers are:

- Simple (lower number of components)
- Cheaper up front cost (as their is less equipment. Although there is a higher cost over time due to increased power losses)

Disadvantages of Half Wave Rectifier

The disadvantages of half-wave rectifiers are:

- They only allow a half-cycle through per sinewave, and the other half-cycle is wasted. This leads to power loss.
- They produces a low output voltage.
- The output current we obtain is not purely DC, and it still contains a lot of ripple (i.e. it has a high ripple factor)

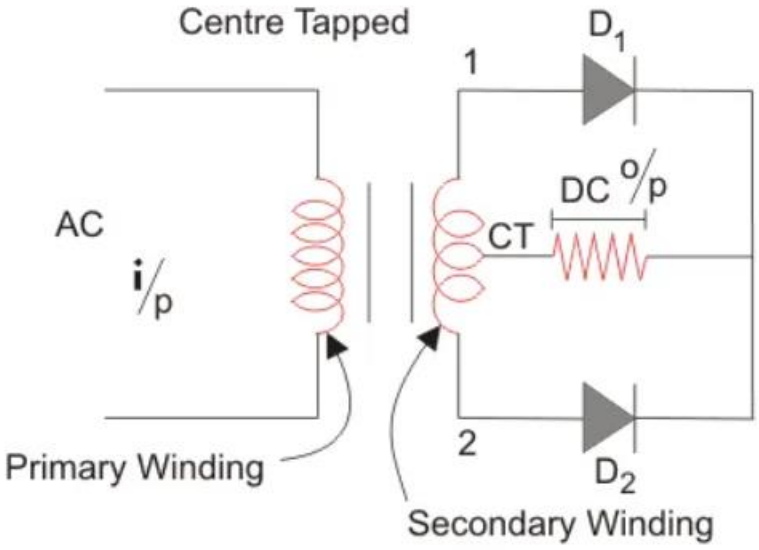
Full Wave Rectifier:

A full wave rectifier is defined as a type of rectifier that converts both halves of each cycle of an alternating wave (AC signal) into a pulsating DC signal. Full-wave rectifiers are used to convert

AC voltage to DC voltage, requiring multiple diodes to construct. Full wave rectification is the process of converting an AC signal to a DC signal.

Circuits that convert alternating current (AC) into direct current (DC) are known as rectifiers. If such rectifiers rectify both the positive and negative half cycles of an input alternating waveform, the rectifiers are full-wave rectifiers.

Full-wave rectifiers achieve this by using a group of diodes. A diode permits current in one direction only and blocks the current in the other direction. We use this principle to construct various rectifiers.



We apply an AC voltage to the input transformer. During the positive half-cycle of the AC voltage, terminal 1 will be positive, centre-tap will be at zero potential, and terminal 2 will be negative potential.

This will lead to forwarding bias in diode D1 and cause current to flow through it. During this time, diode D2 is in reverse bias and will block current through it.

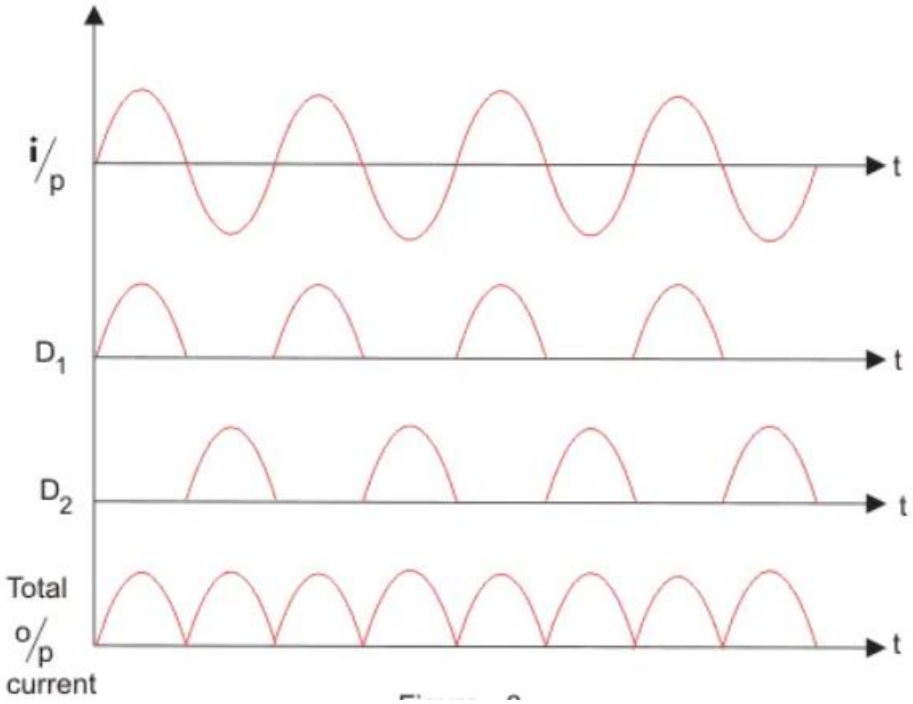
During the negative half-cycle of the input AC voltage, terminal 2 will become positive relative to terminal 2 and centre-tap. This will lead to forwarding bias in diode D2 and cause current to flow through it. During this time, diode D1 is in reverse bias and will block current through it.

During the positive cycle, diode D1 conducts, and during the negative cycle, diode D2 conducts and during the positive cycle.

As a result, both half-cycles are allowed to pass through. The average output DC voltage here is

almost twice the DC output voltage of a half-wave rectifier.

Output Waveforms



Calculations:

Without filter:

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$$

$$V_{dc} = \frac{2V_m}{\pi}$$

Ripple factor (Theoretical) = $\sqrt{(\frac{V_{rms}}{V_{dc}})^2 - 1} = 0.48$

Ripple Factor (Practical) = $\gamma = \frac{V_{ac}}{V_{dc}}$

With filter:

Ripple factor (Theoretical) = $\gamma = \frac{1}{4\sqrt{3}fCR}$

Where f = 50Hz, R =1KΩ, C = 1000μF.

$$V_{ac} = \frac{V_{r(p-p)}}{2\sqrt{3}}$$

$$V_{dc} = V_m - \frac{V_{r(p-p)}}{2}$$

Ripple Factor $\gamma = \frac{V_{ac}}{V_{dc}}$

Percentage Regulation = $(\frac{V_{NL} - V_{FL}}{V_{FL}}) * 100$ %

V_{NL} = DC voltage at the load without connecting the load (Minimum current).

V_{FL} = DC voltage at the load with load connected.

Efficiency $\eta = \frac{P_{DC}}{P_{AC}}$%u200B

$P_{AC} = V_{2rms} / R_L$

$P_{DC} = V_{dc} / R_L$

Advantages of Full Wave Rectifiers:

The advantages of full wave rectifiers include:

- Full wave rectifiers have higher rectifying efficiency than half-wave rectifiers. This means that they convert AC to DC more efficiently.

- They have low power loss because no voltage signal is wasted in the rectification process.
- The output voltage of a centre-tapped full wave rectifier has lower ripples than a halfwave rectifiers.

Disadvantages of Full Wave Rectifiers:

The disadvantages of full wave rectifiers include:

- The centre-tapped rectifier is more expensive than a half-wave rectifier and tends to occupy a lot of space.

Full Wave Bridge Rectifier:

A full wave bridge rectifier is a rectifier that will use four diodes or more than that in a bridge formation. A full wave bridge rectifier system consists of

1. Four Diodes
2. Resistive Load

We use the diodes, namely A, B, C and D, which form a bridge circuit. The circuit diagram is as follows.

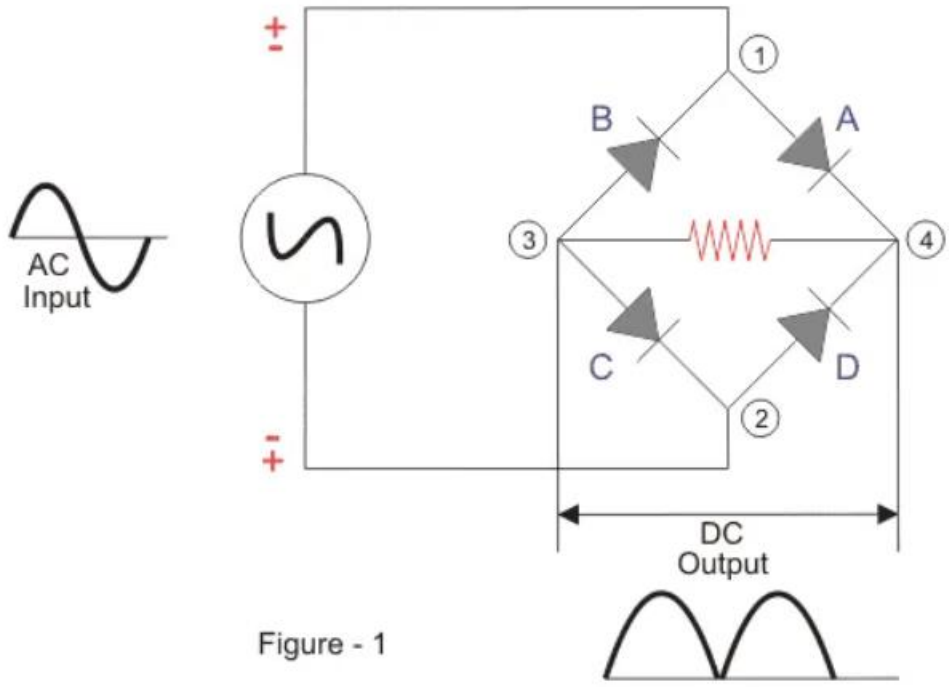


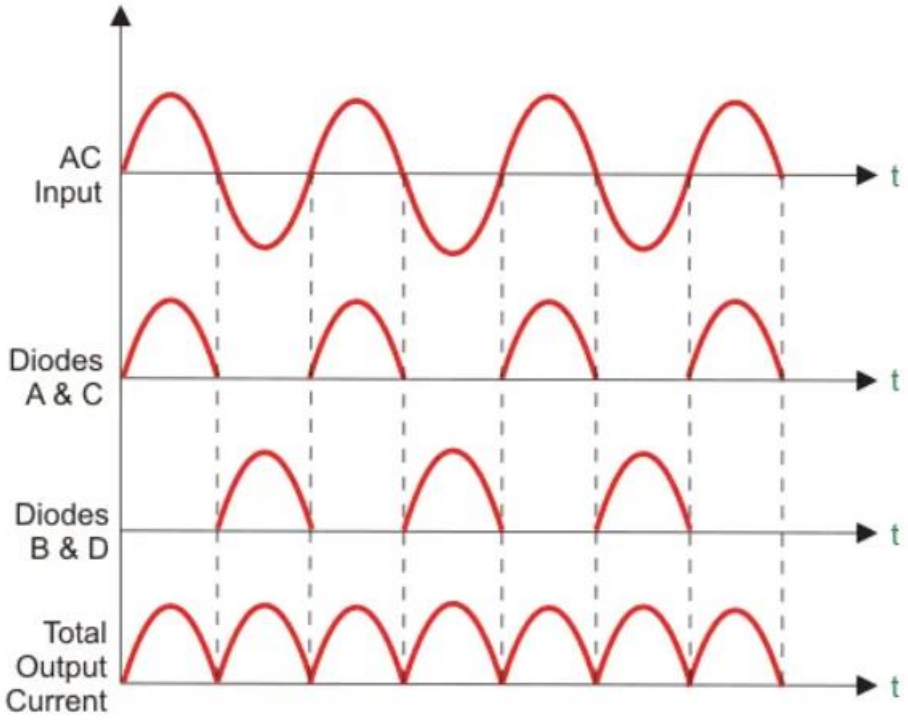
Figure - 1

We apply an AC across the bridge. During the positive half-cycle, terminal 1 becomes positive, and terminal 2 becomes negative.

This will cause the diodes A and C to become forward-biased, and the current will flow through it. Meanwhile, diodes B and D will become reverse-biased and block current through them. The current will flow from 1 to 4 to 3 to 2.

During the negative half-cycle, terminal 1 will become negative, and terminal 2 will become positive.

This will cause the diodes B and D to become forward-biased and will allow current through them. At the same time, diodes A and C will be reverse-biased and will block the current through them. The current will flow from 2 to 4 to 3 to 1.



Advantages of Full Wave Bridge Rectifier:

- The center tap transformer is eliminated.

- The output is double that of the center-tapped full-wave rectifier for the same secondary voltage.
- The peak inverse voltage across each diode is one-half of the center tap circuit of the diode.

Disadvantages of Full Wave Bridge Rectifier:

- It needs four diodes.
- The circuit is not suitable when a small voltage is required to be rectified. It is because, in this case, the two diodes are connected in series and offer double voltage drop due to their internal resistance.

Example:

The full-wave bridge rectifier of 5.7 is supported by a 120 V source. If the load resistance is 10.8 Ω, find,

1. The peak load voltage.
2. The DC voltage across the load.
3. The DC load current.
4. The average current in each diode.
5. The average output power.
6. The rectifier efficiency.
7. The ripple factor.
8. The power factor.

Solution:

1. **Peak load voltage**

   $\mathbf{V_m = \sqrt{2}\, V_{RMS}} = (1.414)\ (120) = 170$ V

2. **DC voltage across the load**

   $V_{o(avg)} = 0.636 \times 170 = 108$ V

3. **DC load current**

   $I_{o(avg)} = 108 / 10.8 = 10$ A

4. **Average current in each diode since the diodes carry the load current alternative half-cycle.**

   $\mathbf{I_{D(avg)} = I_{o(avg)} / 2} = 10 / 2 = 5$ A

5. **Average output power**

   $\mathbf{P_{o(avg)} = V_{o(avg)} \times I_{o(avg)}}$ = 108 x 10 = 1080 W

6. **Rectifier efficiency**

   $\boldsymbol{\eta = 8 / \pi^2}$ = 0.81 or 81%

7. **Ripple factor**

$$RF = \sqrt{\left[\frac{V_{RMS}}{V_{DC}}\right]^2 - 1} = \sqrt{\left[\frac{120}{108}\right]^2 - 1} = 0.482$$

8. **Power factor**

   $\mathbf{PF = P/S = (V_{o(avg)} \times I_{o(avg)}) / (V_{RMS} \times I_{RMS})}$ = (108 x 10) / (120 x 10) = 0.9

Filters:

To remove the AC components or filter them out in a rectifier circuit, a filter circuit is used. A filter circuit is a device to remove the A.C components of the rectified output but allows the D.C components to reach the load. A filter circuit is in general a combination of inductor (L) and Capacitor (C) called LC filter circuit. A capacitor allows A.C only and inductor allows D.C only to pass. So, a suitable L and C network can effectively filter out the A.C component from rectified wave.

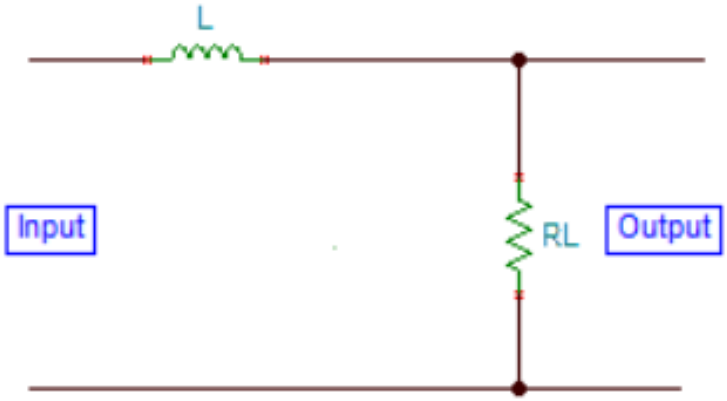
A filter circuit consists of passive circuit elements i.e, inductors, capacitors, resistors, and their combination. The filter action depends upon the electrical properties of passive circuit elements. For example, an inductor allows the D.C to pass through it. But it blocks A.C. On the other hand, a capacitor allows the A.C to pass through it. But it blocks the D.C. Some of the important filters are given below.

Inductor Filter

1. Capacitor Filter
2. LC Filter
3. π Filter

Inductor Filter:

This type of filter is also called choke filter. It consists of an inductor L which is inserted between the rectifier and the load resistance RL. The rectifier contains A.C components as well as D.C components. When the output passes through the inductor, it offers a high resistance to the A.C component and no resistance to D.C components. Therefore, A.C components of the rectified output is blocked and only D.C components reached at the load.

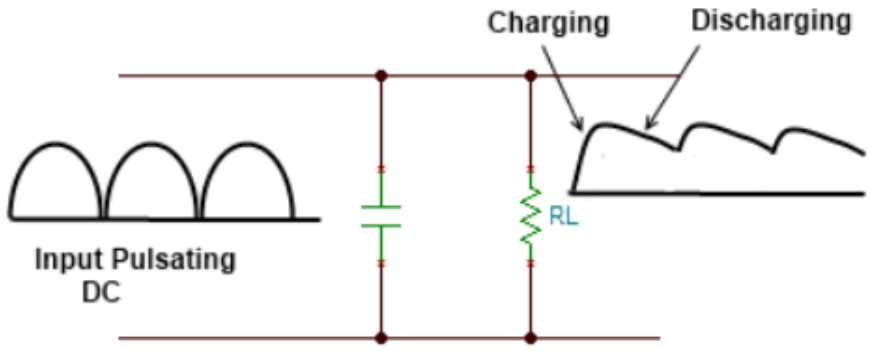


Capacitor Filter:

In consists of a choke in series with the load as shown in the Figure. The Inductor has the inherent characteristic of opposing any change in the current. Hence the introduction of choke in the rectifier circuit will have a smoothing effect. The inductive filter is suitable for heavy loads.

It consists of a capacitor directly across the load as shown in the Figure. At light loads, the capacitor filter maintains the output voltage near to maximum voltage (Vm). The capacitor charges up to the maximum value of input voltage and maintains the value even as the full wave voltage drops to zero.

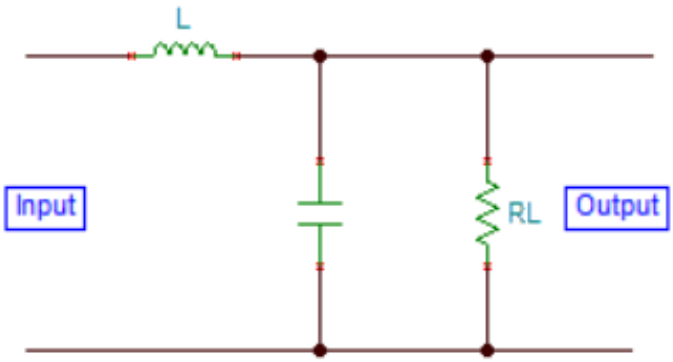
The discharge of capacitor through load resistance takes place till the input voltage raises to a value more than the capacitor voltage. Thus, the diode will again be forward biased causing recharging of capacitor due to diode current. However, as the load increases, the ripple also increases due to the greater discharge of the capacitor.



LC Filter:

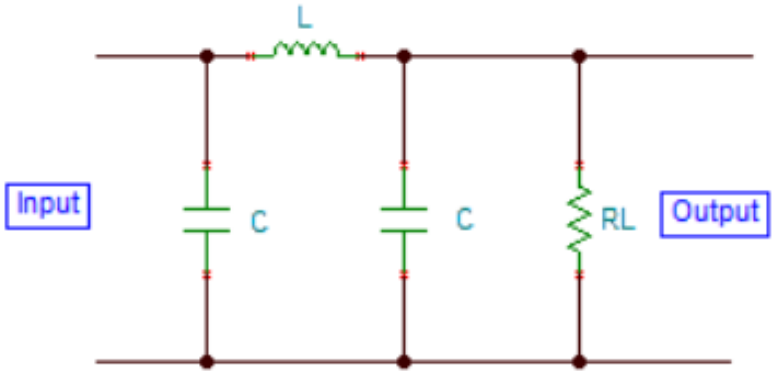
In inductor filter, the ripple factor is directly proportional to the load resistance. On the other hand in a capacitor filter, it is varying inversely with the load resistance. Hence if we combine the inductor filter with the capacitor the ripple factor will become almost independent of the load filter. It is also known as inductor input filter, choke input filter, L input or LC-section.

In this circuit a choke is connected in series with the load. It offers high resistances to the AC components and allows DC component to flow through the load. The capacitor across the load is connected in parallel which filter out any AC component flowing through the choke. In this way the ripples are rectified and a smooth DC is provided through the load.



CLC or P- Filter:

It consists of one inductor and two capacitor connected across its each end. The three components are arranged in shape of Greek letter Pi. It is also called capacitor input Pi filter. The input capacitor C1 is selected to offer very low reactance to the repel frequency hence major parts of filtering is done by C1. Most of the remaining repels are removed by the combining action of L and C2. This circuit gives much better filter then LC filter. However C1 is still directly connected across the supply and would need high pulse of current if load current is large. This filter is used for the low current equipment's.



Section B8: Clippers And Clampers

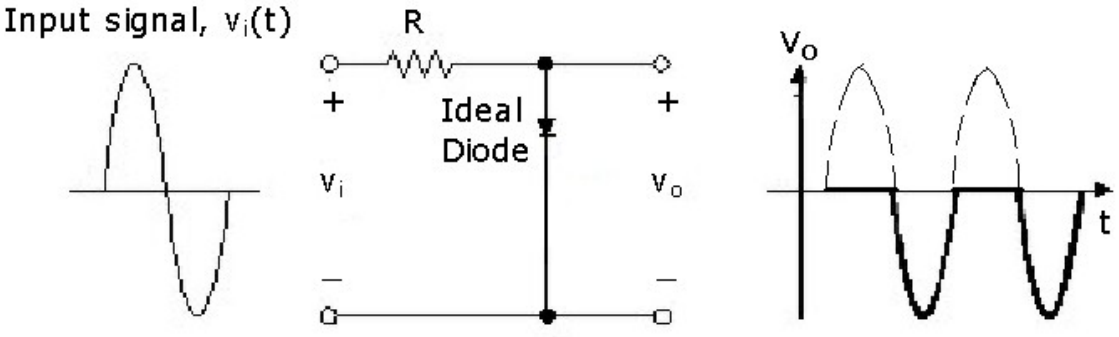
We've been talking about one application of the humble diode – rectification. These simple devices are also powerful tools in other applications. Specifically, this section of our studies looks at signal modification in terms of **clipping** and **clamping**.

Clippers

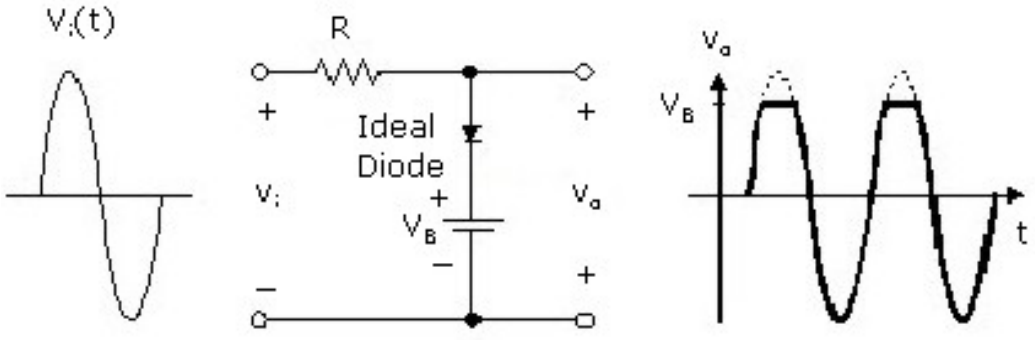
Clipping circuits (also known as **limiters**, **amplitude selectors**, or **slicers**), are used to remove the part of a signal that is above or below some defined reference level. We've already seen an example of a clipper in the half-wave rectifier – that circuit basically cut off everything at the reference level of zero and let only the positive-going (or negative-going) portion of the input waveform through.

To clip to a reference level other than zero, a dc source (shown as a battery in your text) is put in series with the diode. Depending on the direction of the diode and the polarity of the battery, the circuit will either clip the input waveform above or below the reference level (the battery voltage for an ideal diode; i.e., for $V_{on}=0$). This process is illustrated in the four parts of Figure 3.43:

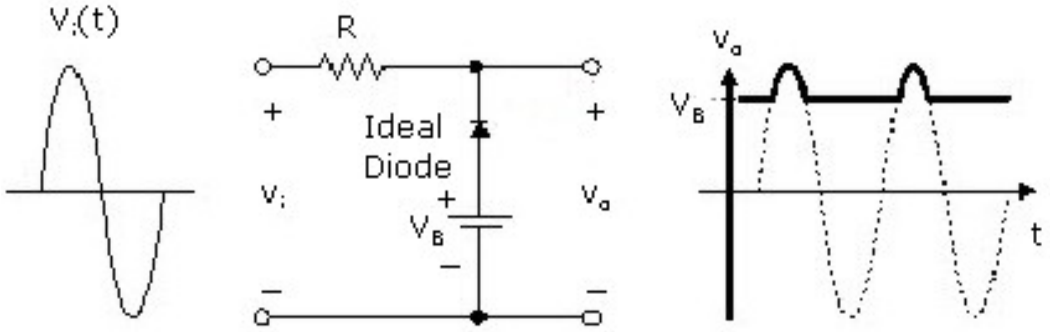
- **Without** the battery, the output of the circuit below would be the negative portion of the input wave (assuming the bottom node is grounded). When $v_i > 0$, the diode is on (short-circuited), v_i is dropped across R and $v_o=0$. When $v_i < 0$, the diode is off (open-circuited), the voltage across R is zero and $v_o=v_i$. (Don't worry; we won't be doing this for ***all*** the circuits!) Anyway, the reference level would be zero.



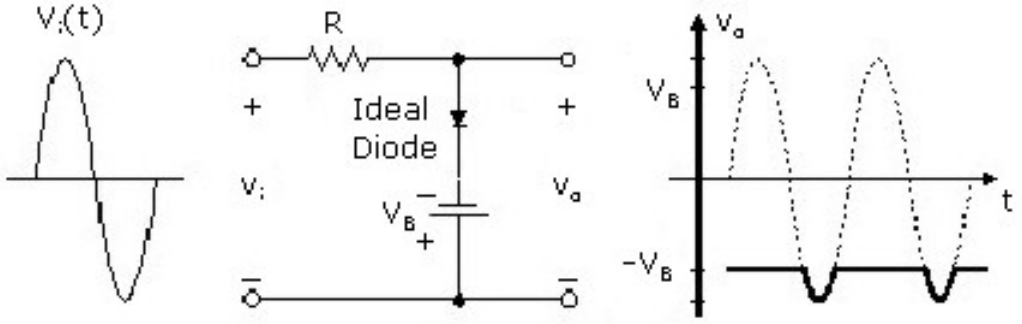
- **With** the battery in the orientation shown in Figure 3.43a (and below), the diode doesn't turn on until $v_i > V_B$ (If this looks strange, revisit the definition of forward bias). This shifts the reference level up and clips the input at $+V_B$ and passes everything for $v_i < V_B$.



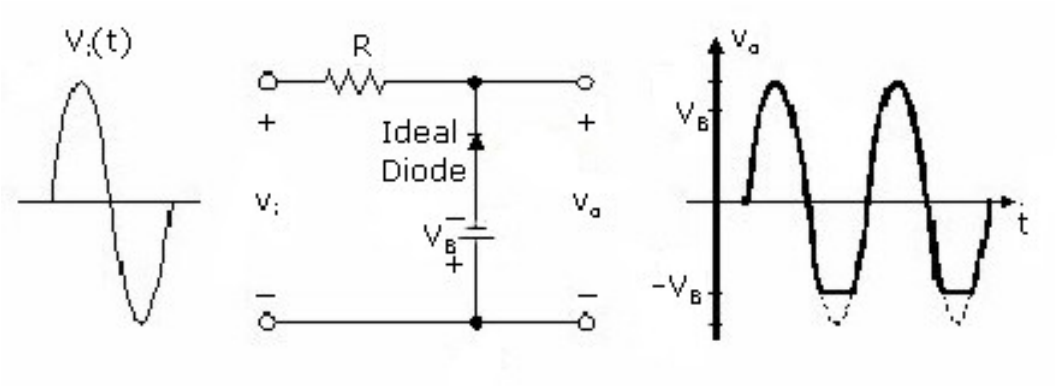
- Figure 3.43b has the battery with the same orientation as in part (a), but the diode has been flipped. **Without** the battery, the positive portion of the input waveform would be passed (i.e., a reference level of zero). **With** the battery, the diode conducts for $v_i < V_B$. This means that the reference level is shifted to $+V_B$ and only $v_i > V_B$ appears at the output.



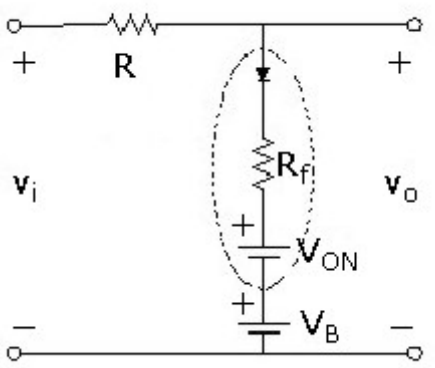
- Again referencing part (a), the diode is in the original position but the polarities on the battery have been switched in Figure 3.43c. The discussion follows the same logic as earlier, but now the reference level has been shifted to $-V_B$. The final result is that $v_o = v_i$ for $v_i < -V_B$.



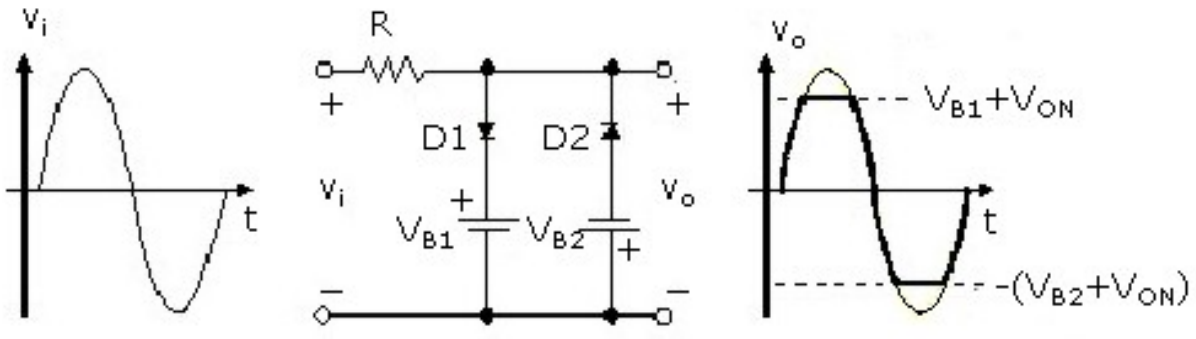
- Finally, Figure 3.43d behaves the same as part (b), but the polarity on the battery has been switched, shifting the reference level to $-V_B$. The signal that appears as the output is v_i as long as $v_i > -V_B$.



To accommodate a practical diode, the turn-on voltage (V_{ON}=0.7V for silicon) and forward resistance (R_f) are included, along with the ideal diode, in the model (as shown in Figure 3.44a, reproduced to the right). The effective reference level will either have a magnitude of V_B+V_{ON} or V_B-V_{ON}, depending on the relative polarities of the two sources (review combining voltage sources in series if necessary). Including R_f in the diode path creates a voltage divider when the diode is forward biased. The result of this slight drop across R_f (remember that the forward resistance is generally pretty small), is a slight distortion in the output waveform – it is no longer strictly "limited" or "clipped" to the reference level, as is illustrated in Figure 3.44b in your text. The four possible configurations of Figure 3.43 are still valid, with the effective reference level ranging in magnitude from 0.7V (if V_B=0) on up.



A **parallel-biased clipper** is a circuit that clips the positive and negative-going portions of the input signal simultaneously. This is designed by using two parallel diodes oriented in opposite directions – note that it is ***very*** important that the diodes are oppositely oriented (think voltage sources in parallel – a big no-no!). Just as in our previous discussion, the path containing diode D1 will provide the upper limit with reference level $V_{B1}+V_{ON}$ (with the V_{B1} polarity shown) and the path containing D2 will provide the lower limit with reference level $V_{B2}+V_{ON}$ (with the V_{B2} polarity shown). An example of this type of clipper, with the resulting output waveform is shown below (Figure 3.45 of your text, where it looks like they assumed R_f was negligible):

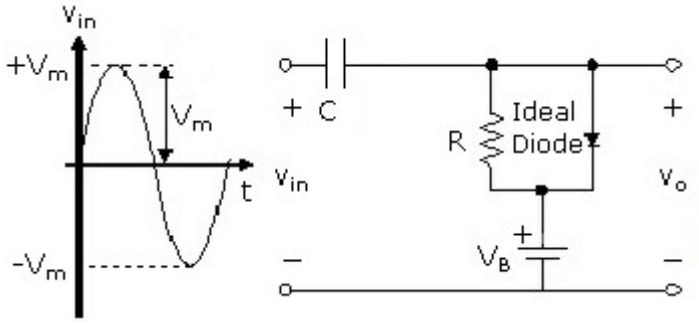


A **series-biased clipper** involves placing a battery in series with the input. The result of this modification is that the input signal is no longer symmetric about the zero axis, but instead shifts by an amount defined by the magnitude and polarity of V_B. In Figure 3.46, the four possible permutations and the resulting output waveforms are shown for an **ideal diode**. When you look at this figure, keep in mind that the input signal is swinging between +2 and –2 volts and the battery magnitude V_B is 1 volt. This may avoid some confusion when looking at the output waveforms – the $(2V+V_B)$ is just 3 volts and the $-(2V-V_B)$ may be replaced by –1 volt. The series placement of the battery is not changing the input waveform in any way, it is simply affecting when the diode turns on. To include the effects of a **practical diode**, include V_{ON} and R_F in the diode path and crunch the math...

Clampers

Clamping circuits, also known as **dc restorers** or **clamped capacitors**, shift an input signal by an amount defined by an independent voltage source. While clippers limit the part of the input signal that reaches the output according to some reference level(s), the entire input reaches the output in a clamping circuit – it is just shifted so that the maximum (or minimum) value of the input is "clamped" to the independent source.

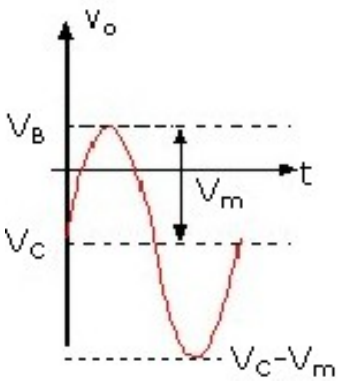
Let's look at Figure 3.48 (input and circuit shown to the right) and see if we can turn this into something that makes sense! Basically, we have a sinusoidal input of magnitude V_m with zero offset (i.e., symmetric signal) fed to the clamper circuit.



Taking the input by sections to build the output…

- If $v_{in} > V_B$, the diode is on, R is shorted, and the output is V_B.
- When $v_{in} < V_B$, the diode is off, current flows through the resistor, and the capacitor charges to a voltage $v_c = V_B - v_{in}$. The maximum voltage on the capacitor will be related to the maximum swing of the input by: $V_C = V_m - V_B$. After fully charging, the capacitor acts like series source in the circuit (with the RC time constant conditions discussed below). After steady state is reached, the output voltage is found by loop analysis as

$$\mathbf{v_o = v_{in} + V_C.}$$

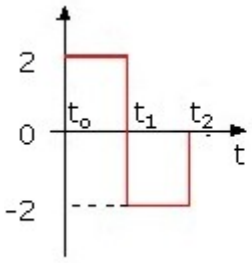


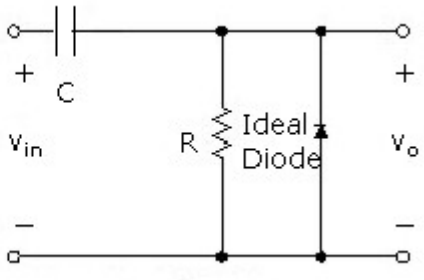
In the circuit shown above, $V_C = -V_m + V_B$ (KVL at maximum negative input, $v_{in}=-V_m$) or $\mathbf{v_o = v_{in} - V_m + V_B}$. Specifically, for the extreme values of the input signal: if $v_{in}=+V_m$, $v_o=V_B$ and if $v_{in}=-V_m$, $v_o=-V_m - V_m + V_B = -V_m - (V_m - V_B) = -V_m + V_C = V_C - V_m$ (Whew! I went through all that to get something that looked like it belonged to the figure to the right!).

Keep in mind that the above analysis was for the diode orientation and V_B polarity shown. If the diode had been flipped, the minimum rather than the maximum of the input would have been clamped to V_B.

A clamping circuit has to have an independent source, a diode, a resistor and a capacitor. To keep a constant voltage on the capacitor over the period of the input, the RC time constant must be large. A **design rule of thumb** is to make the RC time constant at least five times the half-period of the input signal, which results in approximately an 18% error over a half-period due to capacitor discharge. If this error is too large, the RC time constant may be increased but, as with everything in design, there comes a point where factors such as size and power dissipation may make any further improvements impractical.

Following our discussion above for Figure 3.48, Figure 3.49 illustrates a circuit that will clamp a square wave to zero ($V_B=0$).

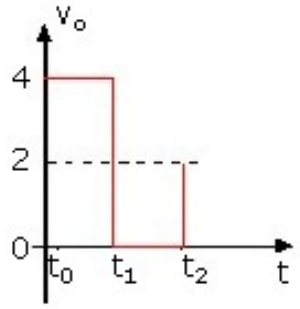




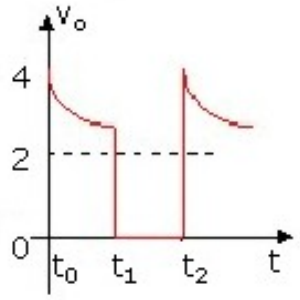
Can you see how this one is working?

$V_C = +V_m = 2V$
(because of diode orientation and $V_B = 0$)
$v_o = v_{in} + V_C$
$v_o = 2\ V_m = 4V$ for $v_{in} = V_m$
$v_o = 0$ for $v_{in} = -\ V_m$

Parts (b) and (c) of this figure, shown below, demonstrate the output of the clamper with a long time constant and the distortion introduced by the capacitor discharging for a short time constant. It is noted in your book that this square wave may be considered a worst-case situation since it places the greatest demands on a clamping circuit due to the instantaneous changes in the waveform. (Remember from your discussions of harmonics and signal composition, that instantaneous change requires infinite frequencies.)



(b) Long time constant



(c) Short time constant

CHAPTER-3
BIPOLAR JUNCTION TRANSISTER (BJT)

Bipolar junction transistors, commonly known as BJT, is a Si or Ge semiconductor device which is structured like two p-n junction diodes connected back to back. It has two outer regions which are the emitter and collector and another region in the middle known as the base. The bipolar junction transistor is called bipolar as both holes and electrons play a fundamental role in its operation.

BJT is a current controlled device, meaning that the current flow through the collector and emitter is controlled by the magnitude of current flowing into the base.

Symbol and terminals in bipolar junction transistor

Emitter: A heavily dope region, that passes charged particles to the base.

Base: A thin and lightly dope region. Base passes the charged particles from the emitter to the collector.

Collector: The largest region of a transistor. It is lightly doped than the emitter but heavily doped than the base. Bipolar junction transistors aid in regulating the current flow in a circuit. The current that flows through the transistor is in proportion to the amount of biasing voltage that is being applied at the base terminal.

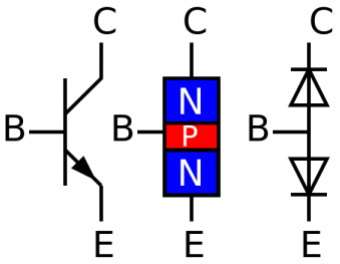


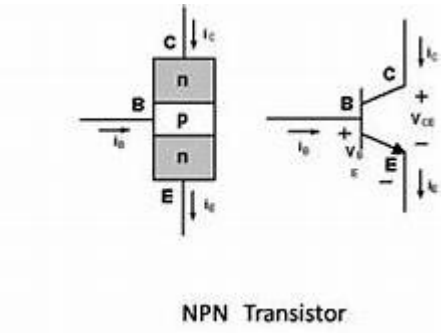
Figure: Typical BJT

Types of Bipolar Junction Transistor and their Operation

Based on their construction, there are two types of BJTs which are the P-N-P and N-P-N types. These two types of structures operate in a similar way. The only difference is their biasing and the polarity of the power supply for each of the structures. The N-type has extra electrons added to it which causes it to become negative. The P-type has electrons removed from it which result in the formation of holes, therefore giving it a positive charge.

NPN Transistor

The **N-P-N** transistors consist of two N- doped semiconductor layers which act as the emitter and collector and a single P-doped layer which acts as the base. A high current is produced in the collector and emitter when the current at the base is amplified.



NPN Transistor

IE, IB and IC are the emitter and collector current and VEB and VCB are the emitter-base and collector base voltages. According to the sign convention, it can be observed that when the current flows into all the terminals the sign of the current is positive. When the current flows out of the emitter terminal and exits the transistor the sign of the current is negative.

A bipolar junction transistor is that it works as an electron valve. When there is no current flowing in the transistor this is because the p-type silicon semiconductor does not have enough electrons which act as a barrier for the conduction of current to take place. The N-P-N bipolar junction transistor will only work when the electrons flow from a region of low electron junction to an area of high electron junction.

An NPN transistor is considered to be in its ON state when the minority carriers in the P-type region allows the electrons to flow between the collector and emitter terminals of the transistor. This allows a large amount of current to flow in the circuit, therefore resulting in faster operation.

The structure of NPN bipolar junction transistor is shown in the figure. It consists of highly doped N type emitter which is surrounded by a P-type lightly doped base. The collector covers the larger portion of the BJT and surrounds the base and the emitter

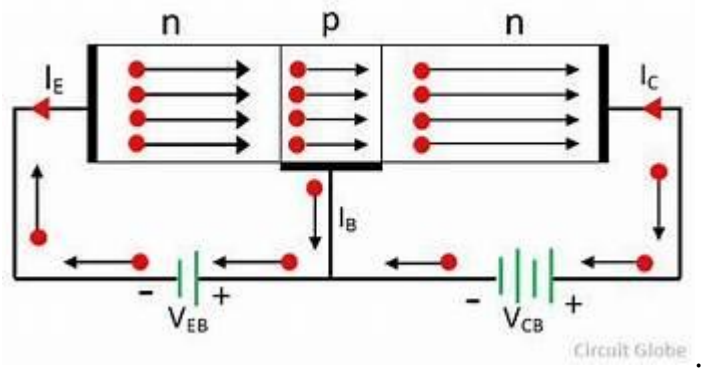
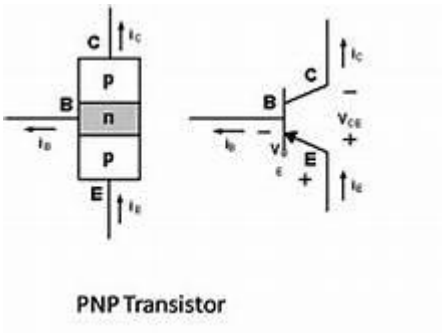


Figure:Construction of NPN transistor

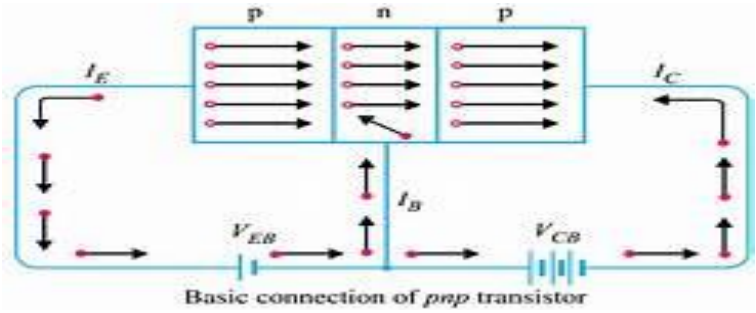
PNP transistor

The **P-N-P** transistor consists of one N-doped semiconductor layer which is the base and two layers of P-doped semiconductor material which act as the collector and emitter. The amplified base current enters the collector at the output. In the P-N-P the current flow is controlled by the base but the current flow is from emitter to collector.



The P-N-P transistor produces a lower current output compared to the N-P-N transistor because instead of electrons, the emitter emits “holes” which denotes the absence of electrons that are collected by the collector. Hence, the transistor operates much slower and is not used as often as the N-P-N transistor.

The structure of PNP bipolar junction transistor is shown in the figure. It consists of highly doped P type emitter which is surrounded by a N-type lightly doped base. The collector covers the larger portion of the BJT and surrounds the base and the emitter.



Working principle of BJT

Since the bipolar junction transistors are made by connecting two diodes back to back, there exists quasi-neutral regions in the emitter, base and collector. These regions remain neutral only at a thermal equilibrium state. This is because when a voltage is supplied the charge densities and electric field in these regions do not change significantly compared to the depletion region. Therefore, for calculating the operation of the BJT these regions are considered neutral. In BJT the emitter to the base junction is forward biased and the collector to the base junction is reverse biased.

When the required voltage is applied to the base, a certain amount of current flows into the base (**IB**). This turns on the transistor and which in turn allows current flow from the collector to the emitter (Assuming that the transistor is NPN type). Let us assume that the base-emitter junction is forward biased and the base-collector junction is reverse biased. The following phenomenon occurs inside the transistor:

- Since the base-emitter junction is forward biased, the positively charged holes from the lightly doped base move through the PN junction to the emitter.
- Also, the forward bias reduces the barrier potential of the base-emitter junction. Hence, a small amount of electrons (nearly 1%) from the emitter crosses the base-emitter junction to reach the lightly doped base and recombines with the holes in the base.
- The remaining electrons in the emitter (about 99%) cross the base-emitter junction and pass through the base-collector junction resulting in electron flow from the emitter to the collector. This constitutes the collector current IB.

IE=IC+ IB

A similar phenomenon occurs in PNP transistor, but the electrons are replaced by holes and holes are replaced by electrons.

Transport factor

The ratio between the collector and emitter current is called the transport factor.

$$\alpha = \frac{I_C}{I_E}$$

Current gain

The ratio between the collector and base current is known as the current gain.

$$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$$

Operation regions of BJT

BJT can act as either insulators or conductors depending on the base current. This gives them the ability to change between two varying states that are switching and amplification. Therefore, the BJT can operate in three operational modes which are:

- Active region: – When the transistor operates in the active region it acts as an amplifier where Ic = β.Ib
- Saturation region: – In this region, the transistor is in a full "ON state" and operates as a switch. Here the collector current is equivalent to the saturation current.
- Cut-Off region: – In the cut-off region the transistor in a full "OFF state" and operates as a switch. No collector current flows through the circuit.
-

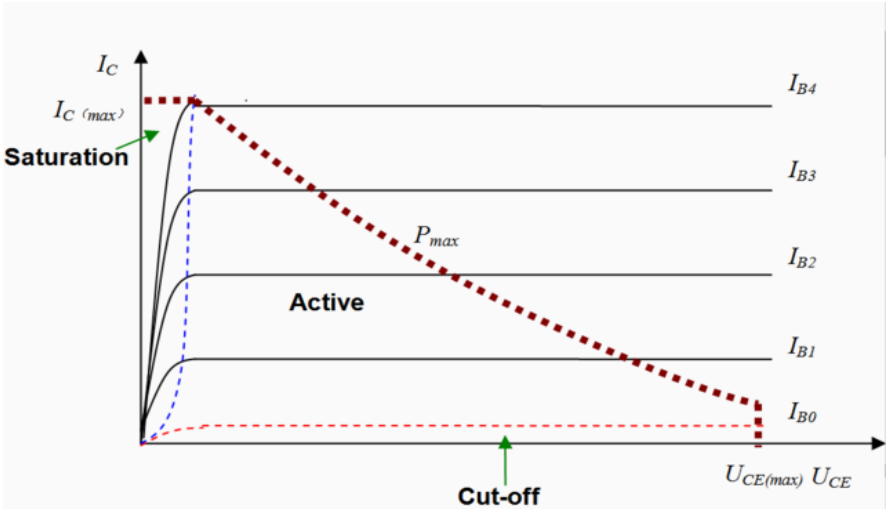


Figure: VI- Characteristics of BJT

The controlled current flows between the emitter and collector and the controlling current flow to the base. Therefore, a small base current controls the larger collector current. When the base has no current flowing through it then it is in a cut off state. When the transistor has maximum current flowing through it then it is said to be in the saturation region and is in a fully conducting state.

The controlled current flows between the emitter and collector and the controlling current flow to the base. Therefore, a small base current controls the larger collector current. When the base has no current flowing through it then it is in a cut off state. When the transistor has maximum current flowing through it then it is said to be in the saturation region and is in a fully conducting state.

Bipolar Transistor Configurations

As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

- **Common Base Configuration** – has Voltage Gain but no Current Gain.
- **Common Emitter Configuration** – has both Current and Voltage Gain.
- **Common Collector Configuration** – has Current Gain but no Voltage Gain.

The Common Base (CB) Configuration

As its name suggests, in the **Common Base** or grounded base configuration, the BASE connection is common to both the input signal AND the output signal. The input signal is applied between the transistors base and the emitter terminals, while the corresponding output signal is taken from between the base and the collector terminals as shown. The base terminal is grounded or can be connected to some fixed reference voltage point.

The input current flowing into the emitter is quite large as its the sum of both the base current and collector current respectively therefore, the collector current output is less

than the emitter current input resulting in a current gain for this type of circuit of “1” (unity) or less, in other words the common base configuration “attenuates” the input signal.

The Common Base Transistor Circuit

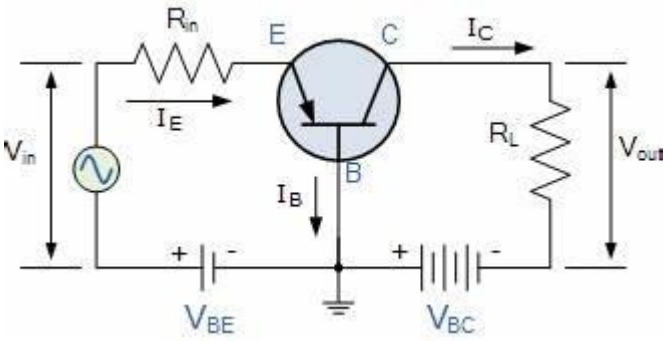


Figure: CB- configuration circuit

This type of amplifier configuration is a non-inverting voltage amplifier circuit, in that the signal voltages Vin and Vout are “in-phase”. This type of transistor arrangement is not very common due to its unusually high voltage gain characteristics. Its input characteristics represent that of a forward biased diode while the output characteristics represent that of an illuminated photo-diode.

Also this type of bipolar transistor configuration has a high ratio of output to input resistance or more importantly “load” resistance (RL) to “input” resistance (Rin) giving it a value of “Resistance Gain”. Then the voltage gain (Av) for a common base configuration is therefore given as:

The Common Emitter (CE) Configuration

In the **Common Emitter** or grounded emitter configuration, the input signal is applied between the base and the emitter, while the output is taken from between the collector and the emitter as shown. This type of configuration is the most commonly used circuit for transistor based amplifiers and which represents the “normal” method of bipolar transistor connection.

The common emitter amplifier configuration produces the highest current and power gain of all the three bipolar transistor configurations. This is mainly because the input impedance is LOW as it is connected to a forward biased PN-junction, while the output impedance is HIGH as it is taken from a reverse biased PN-junction.

The Common Emitter Amplifier Circuit

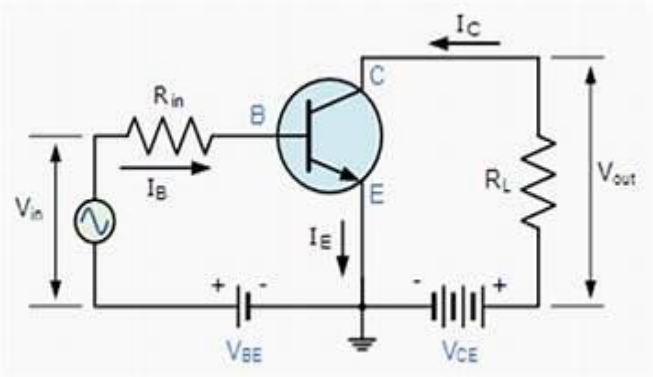


Figure: CE configuration circuit

In this type of configuration, the current flowing out of the transistor must be equal to the currents flowing into the transistor as the emitter current is given as Ie = Ic + Ib.

As the load resistance (RL) is connected in series with the collector, the current gain of the common emitter transistor configuration is quite large as it is the ratio of Ic/Ib. A transistors current gain is given the Greek symbol of Beta, (β).

As the emitter current for a common emitter configuration is defined as Ie = Ic + Ib, the ratio of Ic/Ie is called Alpha, given the Greek symbol of α. Note: that the value of Alpha will always be less than unity.

Since the electrical relationship between these three currents, Ib, Ic and Ie is determined by the physical construction of the transistor itself, any small change in the base current (Ib), will result in a much larger change in the collector current (Ic).

Then, small changes in current flowing in the base will thus control the current in the emitter-collector circuit. Typically, Beta has a value between 20 and 200 for most general purpose transistors. So if a transistor has a Beta value of say 100, then one electron will flow from the base terminal for every 100 electrons flowing between the emitter-collector terminal.

The Common Collector (CC) Configuration

In the **Common Collector** or grounded collector configuration, the collector is connected to ground through the supply, thus the collector terminal is common to both the input and the output. The input signal is connected directly to the base terminal, while the output signal is taken from across the emitter load resistor as shown. This type of configuration is commonly known as a **Voltage Follower** or **Emitter Follower** circuit.

The common collector, or emitter follower configuration is very useful for impedance matching applications because of its very high input impedance, in the region of hundreds of thousands of Ohms while having a relatively low output impedance.

The Common Collector Transistor Circuit

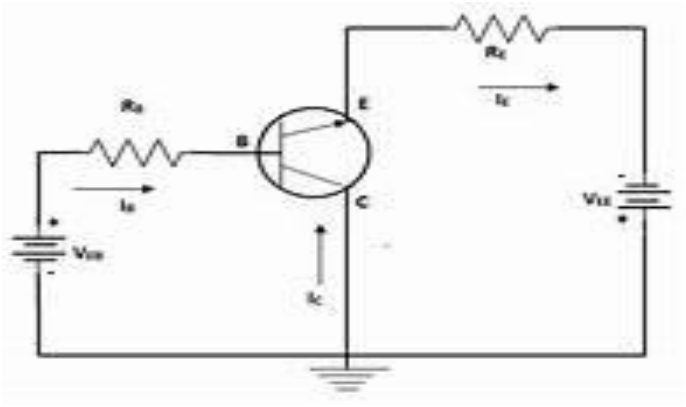


Figure: CC configuration circuit

The common emitter configuration has a current gain approximately equal to the β value of the transistor itself. However in the common collector configuration, the load resistance is connected in series with the emitter terminal so its current is equal to that of the emitter current.

As the emitter current is the combination of the collector AND the base current combined, the load resistance in this type of transistor configuration also has both the collector current and the input current of the base flowing through it.

Characteristic	Common Base	Common Emitter	Common Collector
Input Impedance	Low	Medium	High
Output Impedance	Very High	High	Low
Phase Shift	0^o	180^o	0^o
Voltage Gain	High	Medium	Low
Current Gain	Low	Medium	High
Power Gain	Low	Very High	Medium

Figure: Generalized characteristics of the different transistor configurations.

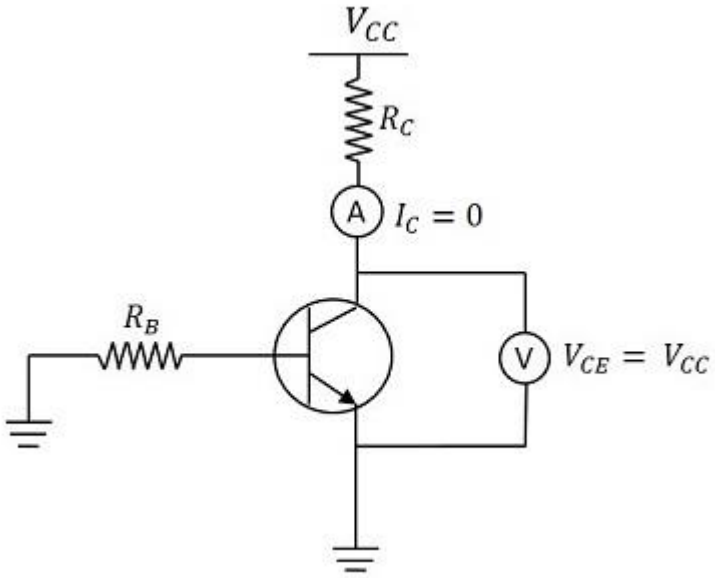
Bipolar Junction Transistor (BJT) Switch

The Bipolar Junction Transistor can be used as a switch. This is required when the typical digital output (max current output 20ma) does not provide sufficient current drive for high current devices like lamps, solenoids or motors. The transistor current gain provides the order of magnitude increase in collector current.

There are two main regions in the operation of a transistor which we can consider as **ON** and **OFF** states. They are saturation and cut **off** states. Let us have a look at the behavior of a transistor in those two states.

Operation in Cut-off condition

The following figure shows a transistor in cut-off region.



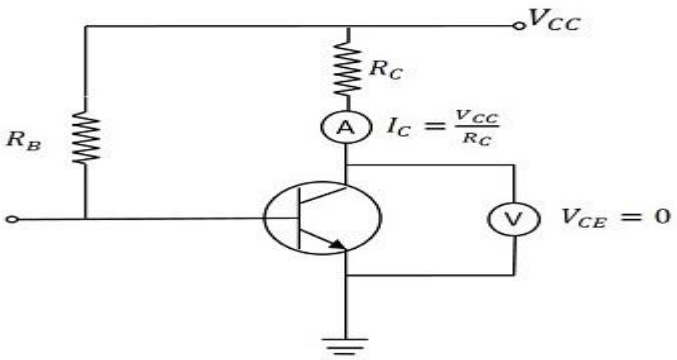
When the base of the transistor is given negative, the transistor goes to cut off state. There is no collector current. Hence IC = 0.

The voltage VCC applied at the collector, appears across the collector resistor RC. Therefore,

VCE = VCC

Operation in Saturation region

The following figure shows a transistor in saturation region.



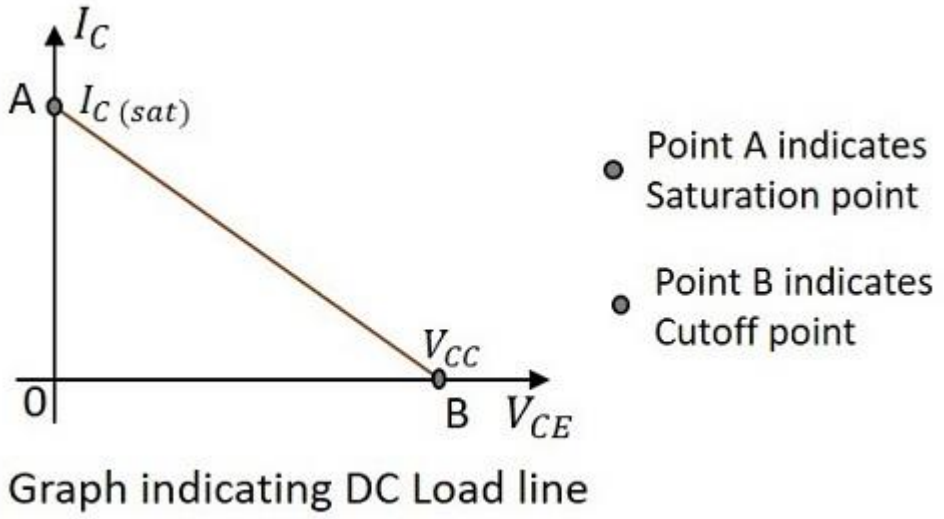
When the base voltage is positive and transistor goes into saturation, IC flows through RC.

Then VCC drops across RC. The output will be zero.

$$I_C = I_{C(sat)} = \frac{V_{CC}}{R_C} \text{ and } V_{CE} = 0 \quad IC = IC(sat) = \frac{VCC}{RC} \text{ and } VCE = 0$$

Actually, this is the ideal condition. Practically, some leakage current flows. Hence we can understand that a transistor works as a switch when driven into saturation and cut off regions by applying positive and negative voltages to the base.

The following figure gives a better explanation.



Graph indicating DC Load line

Observe the dc load line that connects the I_C and V_{CC}. If the transistor is driven into saturation, I_C flows completely and $V_{CE} = 0$ which is indicated by the point **A**.

If the transistor is driven into cut off, IC will be zero and VCE = VCC which is indicated by the point B. the line joining the saturation point A and cut off B is called as **Load line**. As the voltage applied here is dc, it is called as **DC Load line**.

Operating Regions

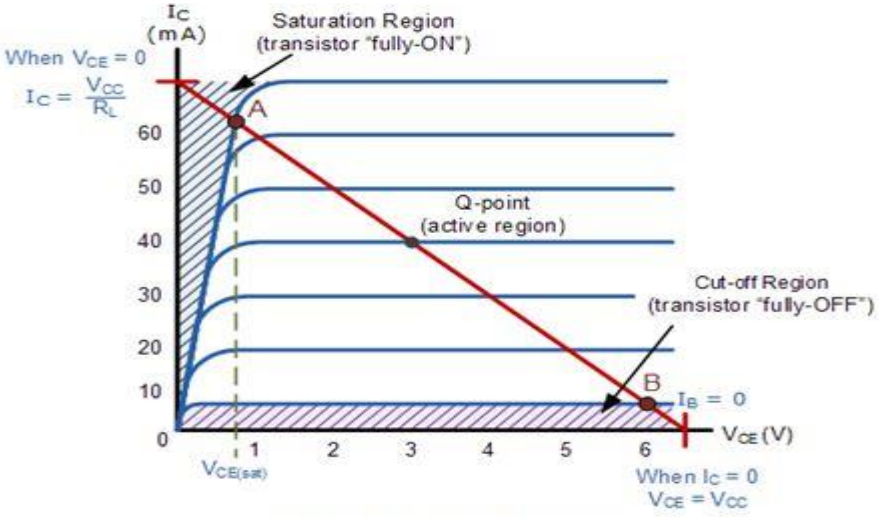


Figure: Operating Regions

The bottom of the curves represents the “Cut-off” region while the area to the left represents the “Saturation” region of the transistor.

Switching Times

The Switching transistor has a pulse as an input and a pulse with few variations will be the output. There are a few terms that you should know regarding the timings of the switching output pulse. Let us go through them.

Let the input pulse duration = **T**

When the input pulse is applied the collector current takes some time to reach the steady state value, due to the stray capacitances. The following figure explains this concept.

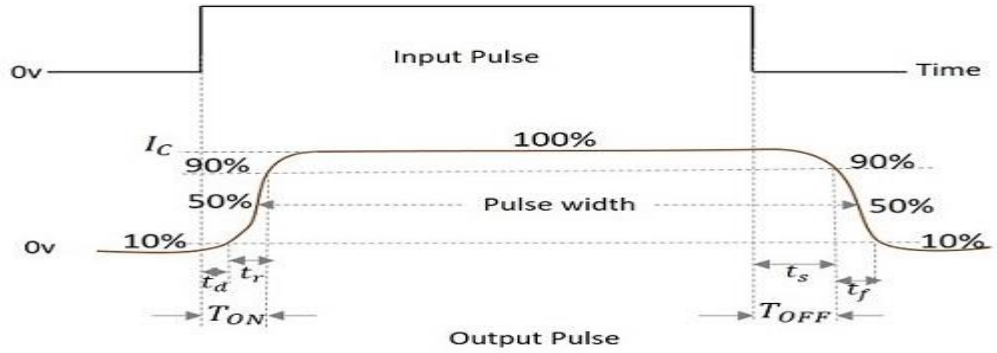


Figure: Transistor switching times

From the figure above,

Time delay(td) − The time taken by the collector current to reach from its initial value to 10% of its final value is called as the **Time Delay**.

Rise time(tr) − The time taken for the collector current to reach from 10% of its initial value to 90% of its final value is called as the **Rise Time**.

Turn-on time (TON) − The sum of time delay (td) and rise time (tr) is called as **Turn-on time**.

$$TON = td + tr$$

Storage time (ts) − The time interval between the trailing edge of the input pulse to the 90% of the maximum value of the output, is called as the **Storage time**.

Fall time (tf) − The time taken for the collector current to reach from 90% of its maximum value to 10% of its initial value is called as the **Fall Time**.

Turn-off time (TOFF) − The sum of storage time (ts) and fall time (tf) is defined as the **Turn-off time**.

$$TOFF = ts + tf$$

Pulse Width(W) − The time duration of the output pulse measured between two 50% levels of rising and falling waveform is defined as **Pulse Width**.

transistor to act as an amplifier, it should be properly biased. We will discuss the need for proper biasing in the next chapter. Here, let us focus how a transistor works as an amplifier.

Transistor Amplifier

A transistor acts as an amplifier by raising the strength of a weak signal. The DC bias voltage applied to the emitter base junction, makes it remain in forward biased condition. This forward bias is maintained regardless of the polarity of the signal. The below figure shows how a transistor looks like when connected as an amplifier.

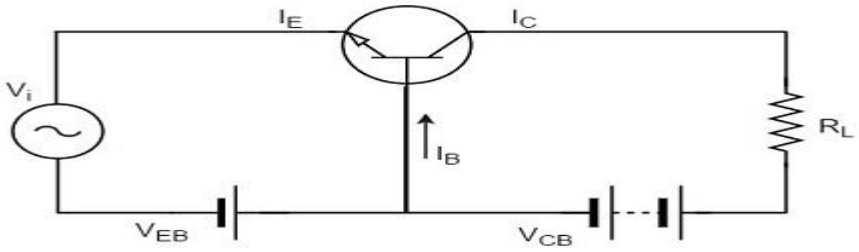


Figure: Transistor as a amplifier

The low resistance in input circuit, lets any small change in input signal to result in an appreciable change in the output. The emitter current caused by the input signal contributes the collector current, which when flows through the load resistor RL, results in a large voltage drop across it. Thus a small input voltage results in a large output voltage, which shows that the transistor works as an amplifier.

Example

Let there be a change of 0.1v in the input voltage being applied, which further produces a change of 1mA in the emitter current. This emitter current will obviously produce a change in collector current, which would also be 1mA.

A load resistance of 5kΩ placed in the collector would produce a voltage of

$5\ k\Omega \times 1\ mA = 5V$

Hence it is observed that a change of 0.1v in the input gives a change of 5v in the output, which means the voltage level of the signal is amplified.

Performance of Amplifier

As the common emitter mode of connection is mostly adopted, let us first understand a few important terms with reference to this mode of connection.

Input Resistance

As the input circuit is forward biased, the input resistance will be low. The input resistance is the opposition offered by the base-emitter junction to the signal flow.

By definition, it is the ratio of small change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage.

Input resistance, $R_i = \Delta V_{BE} / \Delta I_B$

Where R_i = input resistance, V_{BE} = base-emitter voltage, and I_B = base current.

Output Resistance

The output resistance of a transistor amplifier is very high. The collector current changes very slightly with the change in collector-emitter voltage.

By definition, it is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the resulting change in collector current (ΔI_C) at constant base current.

Output resistance = $Ro = \Delta V_{CE} / \Delta I_C Ro$

Where Ro = Output resistance, VCE = Collector-emitter voltage, and IC = Collector-emitter voltage.

Effective Collector Load

The load is connected at the collector of a transistor and for a single-stage amplifier, the output voltage is taken from the collector of the transistor and for a multi-stage amplifier, the same is collected from a cascaded stages of transistor circuit.

By definition, it is the total load as seen by the a.c. collector current. In case of single stage amplifiers, the effective collector load is a parallel combination of RC and Ro.

Effective Collector Load, $R_{AC} = R_C // Ro$

$= RC \times RoRC + Ro = RAC$

Hence for a single stage amplifier, effective load is equal to collector load RC.

In a multi-stage amplifier (i.e. having more than one amplification stage), the input resistance Ri of the next stage also comes into picture.

Effective collector load becomes parallel combination of RC, Ro and Ri i.e,

Effective Collector Load, $RAC = RC // Ro // RiRAC$

$RC // Ri = RCRiRC + Ri$

As input resistance Ri is quite small, therefore effective load is reduced.

Current Gain

The gain in terms of current when the changes in input and output currents are observed, is called as **Current gain**. By definition, it is the ratio of change in collector current (ΔIC) to the change in base current (ΔIB).

Current gain, $\beta = \Delta I_C / \Delta I_B$

The value of β ranges from 20 to 500. The current gain indicates that input current becomes β times in the collector current.

Voltage Gain

The gain in terms of voltage when the changes in input and output currents are observed, is called as **Voltage gain**. By definition, it is the ratio of change in output voltage (ΔVCE) to the change in input voltage (ΔVBE).

Voltage gain, $AV=\Delta V_{CE}/\Delta V_{BE}$

$=Changeinoutputcurrent\times effectiveloadChangeininputcurrent\times input\ resistance=Changeinoutputcurrent\times effectiveloadChangeininputcurrent\times input\text{-}resistance$

$=(\Delta I_c\times R_{ac})/(\Delta I_b\times Ri)=(\Delta I_c/\Delta I_b)\times(R_{AC}/Ri)=\beta\times R_{AC}Ri$

For a single stage, RAC = RC.

However, for Multistage,

$RAC=(R_C\times Ri)/(R_C+R_I)$

Where Ri is the input resistance of the next stage.

Power gain

The gain in terms of power when the changes in input and output currents are observed, is called as **Power gain**.

By definition, it is the ratio of output signal power to the input signal power.

Power gain, $Ap=(\Delta I_C/\Delta I_B)^2\times(R_{AC}/Ri)$

= Current gain × Voltage gain

Hence these are all the important terms which refer the performance of amplifiers.

Transistor Characteristics

Transistor Characteristics are the plots which represent the relationships between the current and the voltages of a transistor in a particular configuration. By considering the transistor configuration circuits to be analogous to two-port networks, they can be analyzed using the characteristic-curves which can be of the following types

1. Input Characteristics: These describe the changes in input current with the variation in the values of input voltage keeping the output voltage constant.
2. Output Characteristics: This is a plot of output current versus output voltage with constant input current.
3. Current Transfer Characteristics: This characteristic curve shows the variation of output current in accordance with the input current, keeping output voltage constant.

Common Base (CB) Configuration of Transistor

In CB Configuration, the base terminal of the transistor will be common between the input and the output terminals as shown by Figure 1. This configuration offers low input impedance, high output impedance, high resistance gain and high voltage gain.

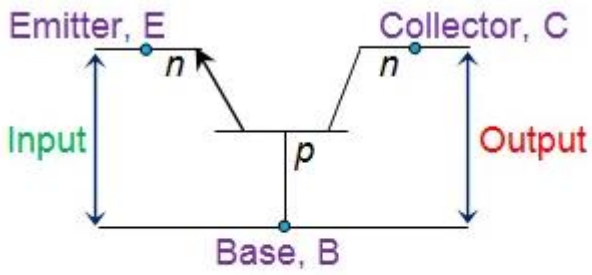


Figure: Common Base configuration

Input Characteristics for CB Configuration of Transistor

Figure below shows the input characteristics of a CB configuration circuit which describes the variation of emitter current, IE with Base-Emitter voltage, VBE keeping Collector-Base voltage, VCB constant.

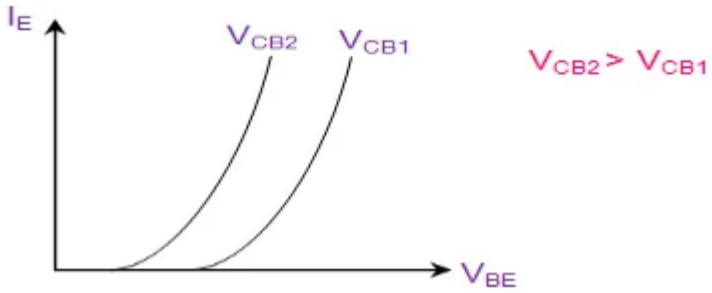


Figure: Input characteristics of CB configuration

This leads to the expression for the input resistance as

$$R_{in} = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{V_{CB}=constant}$$

Output Characteristics for CB Configuration of Transistor

The output characteristics of CB configuration (Figure) show the variation of collector current, IC with VCB when the emitter current, IE is held constant. From the graph shown, the output resistance can be obtained as:

$$R_{out} = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E=constant}$$

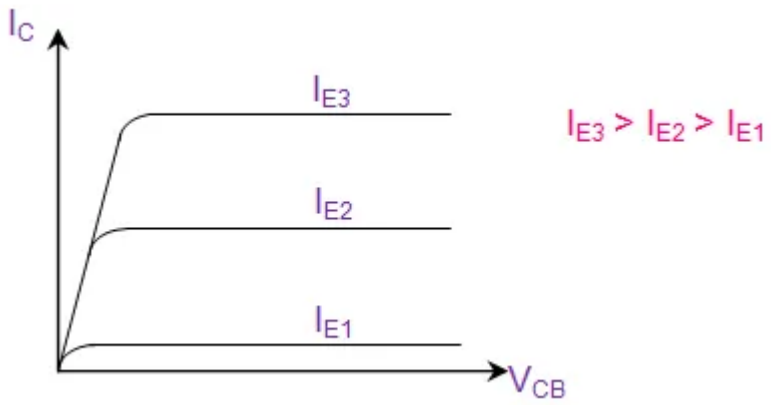


Figure: Output characteristics of CB configuration

Current Transfer Characteristics for CB Configuration of Transistor

Figure below shows the current transfer characteristics for CB configuration which illustrates the variation of IC with the IE keeping VCB as a constant. The resulting current gain has a value less than 1 and can be mathematically expressed as:

$$\alpha = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=constant}$$

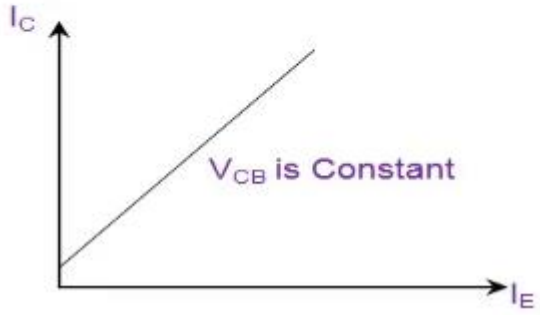


Figure:Current transfer characteristics of CB configuration

Common Collector (CC) Configuration of Transistor

This transistor configuration has the collector terminal of the transistor common between the input and the output terminals (Figure) and is also referred to as emitter follower configuration. This offers high input impedance, low output impedance, voltage gain less than one and a large current gain.

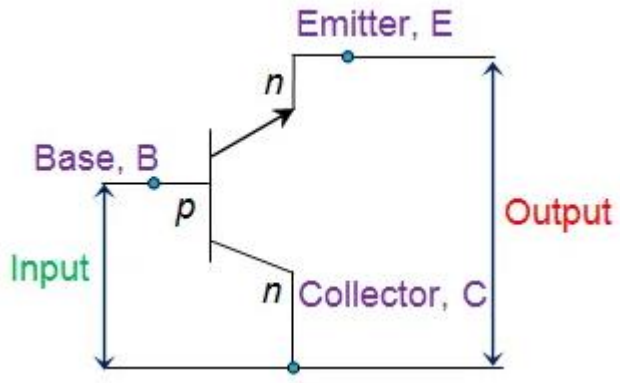


Figure: Common Collector configuration

Input Characteristics for CC Configuration of Transistor

Figure shows the input characteristics for CC configuration which describes the variation in IB in accordance with VCB, for a constant value of Collector-Emitter voltage, VCE.

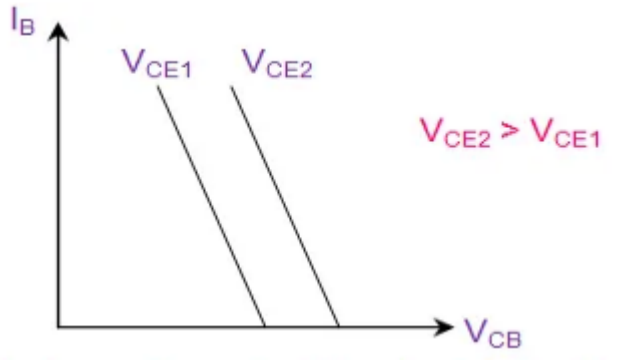


Figure: input characteristics of CC configuration

Output Characteristics for CC Configuration of Transistor

Figure below shows the output characteristics for the CC configuration which exhibit the variations in IE against the changes in VCE for constant values of IB.

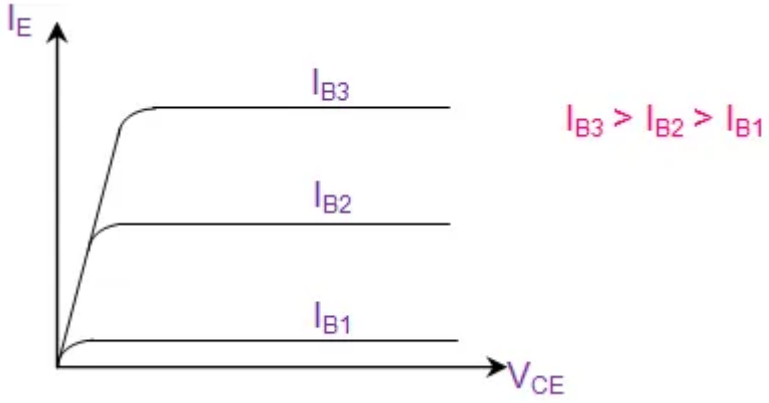


Figure : Output characteristics of CC configuration

Current Transfer Characteristics for CC Configuration of Transistor

This characteristic of CC configuration (Figure) shows the variation of IE with IB keeping VCE as a constant.

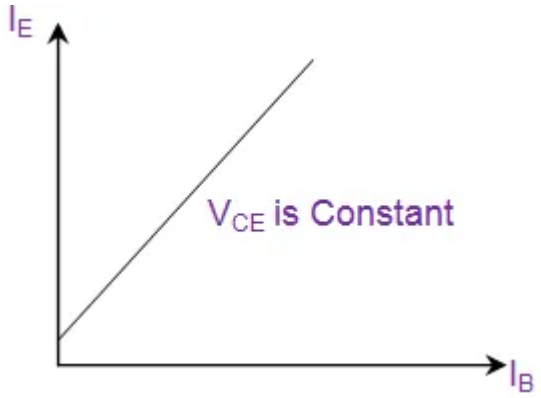


Figure: Current transfer characteristics of CC configuration

Common Emitter (CE) Configuration of Transistor

In this configuration, the emitter terminal is common between the input and the output terminals as shown by Figure . This configuration offers medium input impedance, medium output impedance, medium current gain and voltage gain.

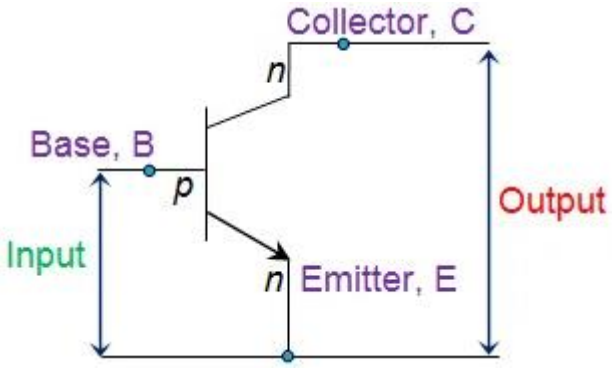


Figure: Common Collector configuration

Input Characteristics for CE Configuration of Transistor

Figure shows the input characteristics for the CE configuration of transistor which illustrates the variation in IB in accordance with VBE when VCE is kept constant.

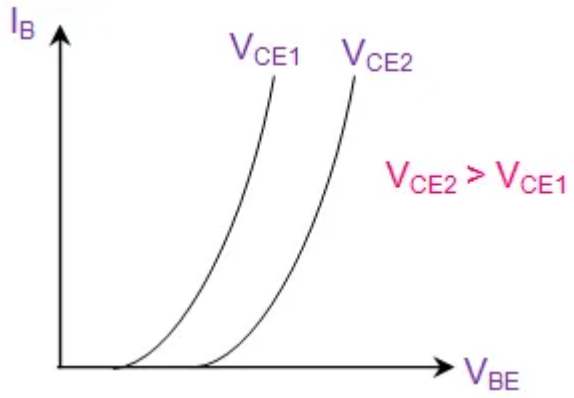


Figure : Input characteristics of CE configuration

From the graph shown in Figure above, the input resistance of the transistor can be obtained as

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_B}\Big|_{V_{CE}=constant}$$

Output Characteristics for CE Configuration of Transistor

The output characteristics of CE configuration (Figure) are also referred to as collector characteristics. This plot shows the variation in IC with the changes in VCE when IB is held constant. From the graph shown, the output resistance can be obtained as:

$$R_{out} = \frac{\Delta V_{CE}}{\Delta I_C}\Big|_{I_B=constant}$$

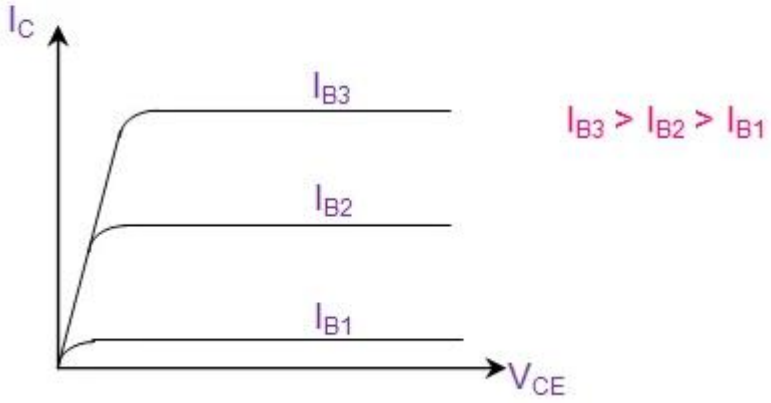


Figure : Output characteristics of CE configuration

Current Transfer Characteristics for CE Configuration of Transistor

This characteristic of CE configuration shows the variation of IC with IB keeping VCE as a constant. This can be mathematically given by

$$\beta = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE}=constant}$$

This ratio is referred to as common-emitter current gain and is always greater than 1.

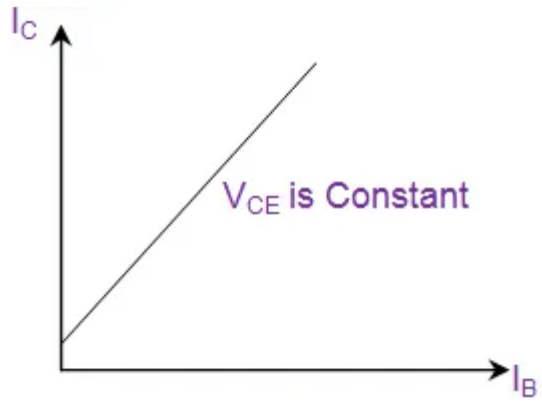


Figure: Current transfer characteristics of CE configuration

Early effect phenomena of a BJT

We have heard many times the Early effect phenomena of a BJT, but what is it. So, here in this article we will discuss about the Early Effect Phenomena of a Bipolar Junction Transistor in detail.

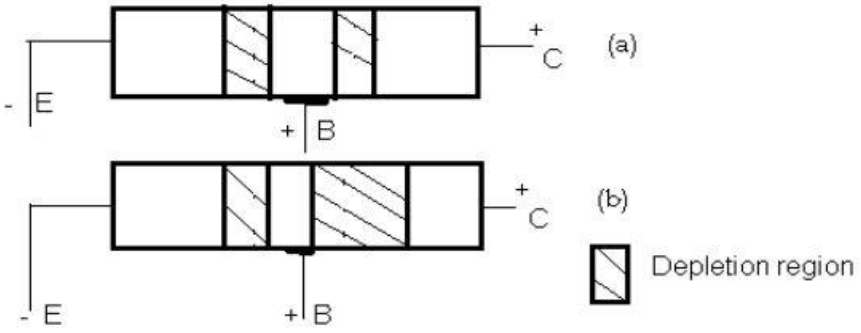


Figure: Early effect in bjt

The transition region at a junction is the region of uncovered charges on both sides of the junction at the positions occupied by the impurity atoms. As the voltage applied across the Common-Base junction increases, the transition region penetrates deeper into the collector and base. Since the doping in the base is lower than that of the Collector, therefore the penetration of the transition region into the base is much larger than into the collector. As a result the electrical base width of the transistor is reduced in comparison to metallurgical base width. This modulation of the effective base width by the collector voltage is known as the Early Effect, named after J.M. EARLY, who first interpreted the early effect phenomena.

This decrease of the base width with increasing reverse collector voltage has some consequences such as:

- There is less chance for recombination within the base region.
- The concentration gradient of minority charge carriers is increased within the base. Since the hole current injected across the emitter is proportional to the gradient of the minority carriers at the emitter junction, the Emitter-current increases with increasing reverse collector voltage.
- For the extremely large voltages, base width may be reduced to zero causing the voltage to breakdown in the transistor. This phenomena is known as punch through or reach through effect.

Transistor parameters:

A transistor is a three-terminal semiconductor device that is used for amplification and switching purposes in an electronic circuit. Out of the three terminals, one pair of terminals is used to supply the input voltage/current, and the other pair of terminals is used to obtain the controlled output current/voltage.

There are thousands of transistor available in the market today. The transistor parameters help us choose the best transistor that is needed for the required application.

Some of the important parameters of transistors are mentioned below:

Current gain

The current gain of a transistor is the measure of the ability of the transistor's amplification property. It is usually denoted by β or hfe. The current gain is the ratio of the base current to the collector current.

Collector-Emitter Voltage (VCEO)

VCEO is the maximum voltage that a collector-emitter junction voltage that a transistor can handle. For most transistors, the VCEO is 30 V.

Emitter-Base Voltage (VEBO)

VEBO is the measure of the maximum voltage that can be applied across the emitter-base voltage. VEBO is relatively smaller than VCEO.

Collector current (IC)

Ic is the measure of the maximum current that can flow through the collector. This current is generally defined in milliamps.

Current Amplification Factor (γ)

The ratio of change in emitter current (ΔIE) to the change in base current (ΔIB) is known as **Current Amplification factor** in common collector (CC) configuration. It is denoted by γ.

$$\gamma = \Delta IE / \Delta IB$$

- The current gain in CC configuration is same as in CE configuration.
- The voltage gain in CC configuration is always less than 1.

Relation between γ and α

Let us try to draw some relation between γ and α

$$\gamma=\Delta I_E/\Delta I_B$$

$$\alpha=\Delta I_C/\Delta I_E$$

$$I_E=I_B+I_C$$

$$\Delta I_E=\Delta I_B+\Delta I_C$$

$$\Delta I_B=\Delta I_E-\Delta I_C$$

Substituting the value of IB, we get

$$\gamma=\Delta I_E/(\Delta I_E-\Delta I_C)$$

Dividing by ΔI_E

$$\gamma=(\Delta I_E/\Delta I_E)/(\Delta I_E/\Delta I_E)-(\Delta I_C/\Delta I_E)$$

$$=1/1-\alpha$$

$$\gamma=1/1-\alpha$$

Expression for collector current

We know

$$I_C=\alpha I_E+I_{CBO}$$

$$I_E=I_B+I_C=I_B+(\alpha I_E+I_{CBO})$$

$$I_E=(1-\alpha)=I_B+I_{CBO}$$

$$I_E=I_B(1-\alpha)+I_{CBO}/(1-\alpha)$$

$$I_C\cong I_E=(\beta+1)I_B+(\beta+1)I_{CB0}$$

Relationship between amplification factors α and β

using $\beta = \frac{I_C}{I_B}$, $\alpha = \frac{I_C}{I_E}$

and $I_E = I_C + I_B$

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta} \rightarrow \frac{1}{\alpha} = 1$$

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

$$\boldsymbol{\alpha = \frac{\beta}{\beta + 1}} \qquad \boldsymbol{\beta = \frac{\alpha}{\alpha - 1}}$$

Reach Through, or Punch – Through Condition

As the voltage applied across the junction increases, the transition region penetrated deep into the base. Since the base is very thin, it is possible that, at moderate voltages, the transition region will have spread completely across the base to reach emitter junction.

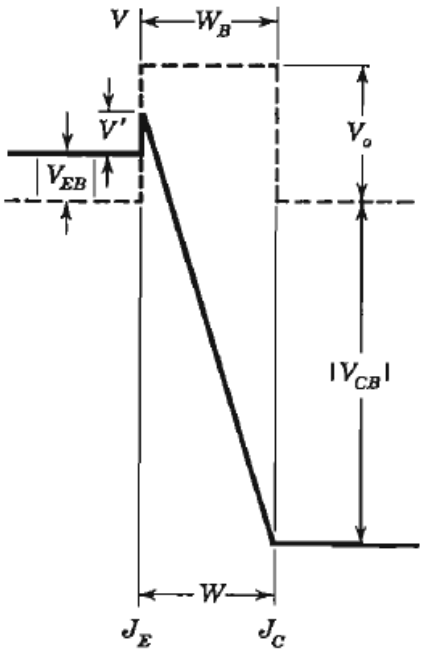


Figure:Potential Variation across transistor sections

The emitter barrier is now V', which is smaller than V0 – |VEB| because the the collector voltage has **'Reached Through' the base region.** This lowering of the emitter – junction voltage may result in an excessively large emitter current, thus placing an upper limit on the magnitude of the collector voltage.

Reach Through differs from Avalanche Breakdown in that it takes place at a fixed voltage between collectors and base , and is not dependent on circuit configuration. Ina particular transistor the voltage limit is determined by these two phenomena , whichever occurs at the lower voltage.

Typical Transistor junction voltage values

Transistor	Vce sat	Vbe sat	Vbe active	Vbe cut-in	Vbe cut-off
Si	0.2 V	0.8 V	0.7 V	0.5 V	0 V
Ge	0.1 V	0.3 V	0.2 V	0.1 V	-0.1 V

- In the saturation region $I_c > \beta I_b$
- For active region $V_{ce} > V_{ce(sat)}$

UNIT IV
BJT BIASING AND THERMAL STABILITY

CONTENT:

Need for Biasing, Operation point, Load Line Analysis – D.C. Load Line, A.C Load Line, and Biasing - Methods, Basic Stability, Fixed Bias, Collector-to-base and self-Bias.

Biasing

Biasing is the process of providing DC voltage which helps in the functioning of the circuit. A transistor is based in order to make the emitter base junction forward biased and collector base junction reverse biased, so that it maintains in active region, to work as an amplifier.

In the previous chapter, we explained how a transistor acts as a good amplifier, if both the input and output sections are biased.

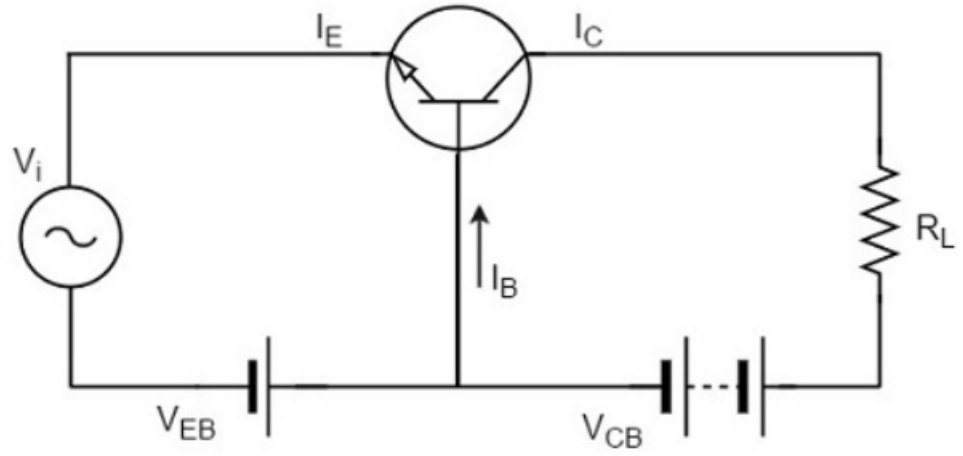
Need for Biasing?

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed **cut-in voltage** for the transistor to be **ON**.
- The BJT should be in the **active region**, to be operated as an **amplifier**.

If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this problem can be avoided. The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed.

The below figure shows a transistor amplifier that is provided with DC biasing on both input and output circuits.

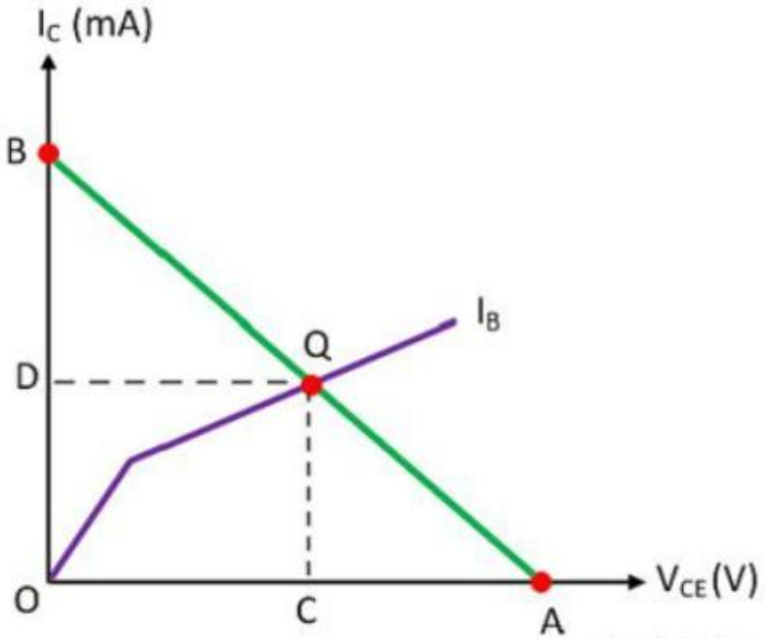


For a transistor to be operated as a faithful amplifier, the operating point should be stabilized. Let us have a look at the factors that affect the stabilization of operating point.

Operating Point

The point which is obtained from the values of the IC (collector current) or VCE (collector-emitter voltage) when no signal is given to the input is known as the operating point or Q-point in a transistor. It is called operating point because variations of IC (collector current) and VCE (collector-emitter voltage) takes place around this point when no signal is applied to the input.

The operating point is also called quiescent (silent) point or simply Q-point because it is a point on IC – VCE characteristic when the transistor is silent, or no input signal is applied to the circuit. The operating point can be easily obtained by the DC load line method. The DC load line is explained below.



Let, determines the operating point of particular base circuit current I_B. According to the load line condition, the OA = V_{CE} = V_{CC} and OB = I_C = V_{CC}/R_C is shown on the output characteristic curve above. The point Q is the operating point where the DC load line intersects the base current I_B at the output characteristic curves in the absence of input signal.

Where I_C= OD mA

V_{CE} = OC volts.

The position of the Q-point depends on the applications of the transistor. If the transistor is used as a switch, then for open switch the Q-point is in the cutoff region, and for the close switch, the Q-point is in the saturation region. The Q-point lies in the middle of the line for the transistor which operates as an amplifier.

Note: In saturation region, both the collector base region and the emitter-base region are in forward biased and heavy current flow through the junction. And the region in which both the junctions of the transistor are in reversed biased is called the cut-off region.

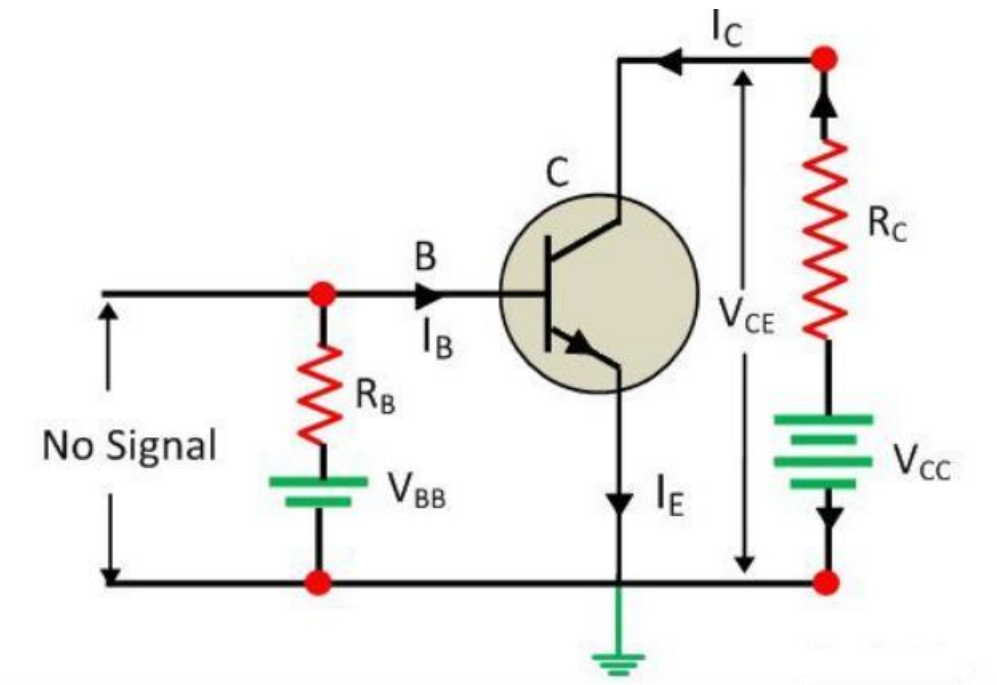
Load Line Analysis

The load line analysis of transistor means for the given value of collector-emitter voltage we find the value of collector current. This can be done by plotting the output characteristic and then determine the collector current IC with respect to collector-emitter voltage VCE. The load line analysis can easily be obtained by determining the output characteristics of the load line analysis methods.

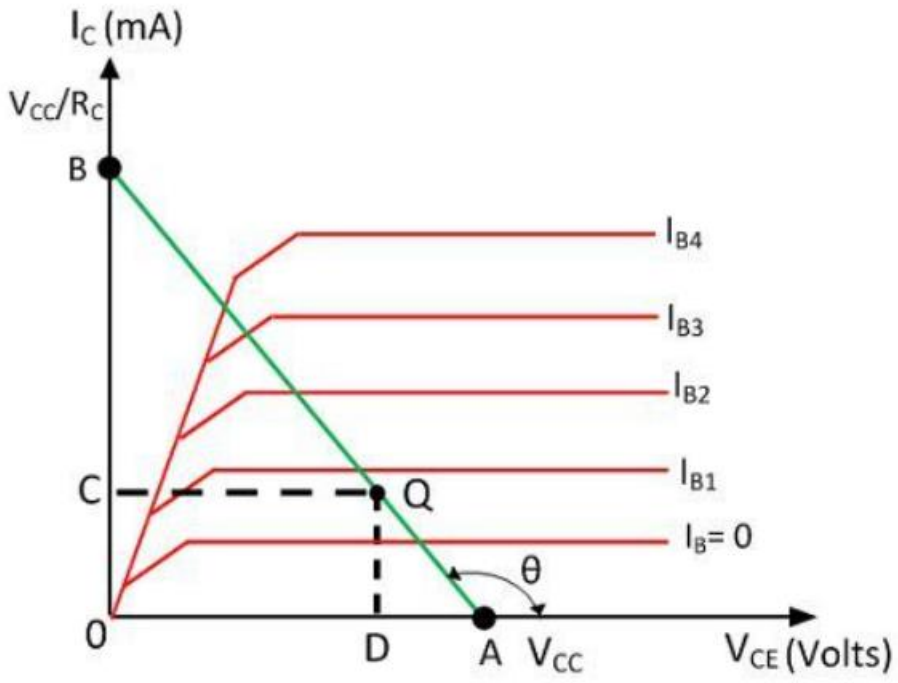
D.C. Load Line Analysis:

The DC load represents the desirable combinations of the collector current and the collector-emitter voltage. It is drawn when no signal is given to the input, and the transistor becomes bias.

Consider a CE NPN transistor circuit shown in the figure below where no signal is applied to the input side. For this circuit, DC condition will obtain, and the output characteristic of such a circuit is shown in the figure below.



The DC load line curve of the above circuit is shown in the figure below.



By applying Kirchhoff's voltage law to the collector circuit, we get,

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C \ldots . equ(1)$$

The above equation shows that the V_{CC} and R_C are the constant value, and it is the first-degree equation which is represented by the straight line on the output characteristic. This load line is known as a DC load line. The input characteristic is used to determine the locus of V_{CE} and I_C point for the given value of R_C. The end point of the line are located as

1. The collector-emitter voltage V_{CE} is maximum when the collector current $I_C = 0$ then from the equation (1) we get,

$$V_{CE} = V_{CC} - 0 \times R_C$$

$$V_{CE} = V_{CC}$$

The first point A (OA = V_{CC}) on the collector-emitter voltage axis shown in the figure above.

2. The collector current I_C becomes maximum when the collector-emitter voltage $V_{CE} = 0$ then from the equation (1) we get.

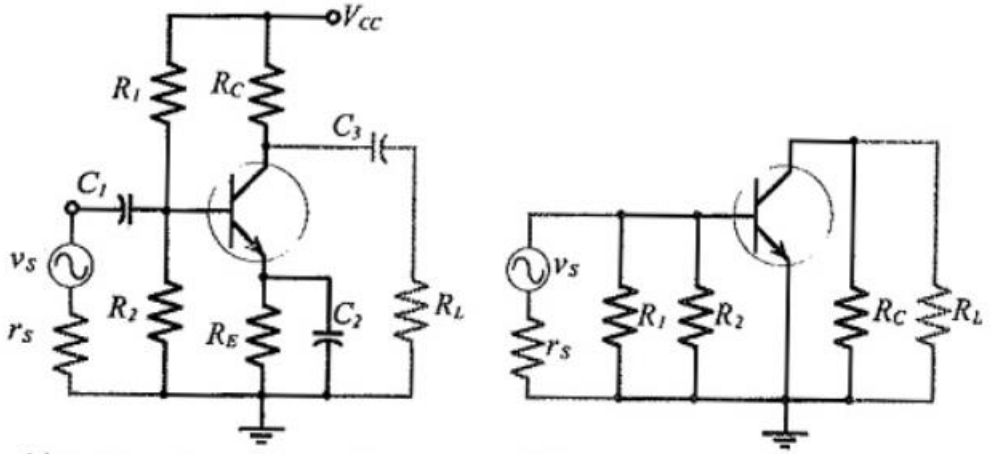
$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C}$$

This gives the second point on the collector current axis as shown in the figure above.
By adding the points A and B, the DC load line is drawn. With the help of load line, any value of collector current can be determined.

AC Load Line

AC Equivalent Circuits – Capacitors behave as short-circuits to ac signals, so in the ac equivalent circuit for a transistor circuit all capacitors must be replaced with short-circuits. Power supplies also behave as ac short-circuits, because the dc supply voltage is not affected by ac signals. Also, all power supplies have large-value capacitors at the output terminals, and these will offer short-circuits to ac signals. Substituting short-circuits in place of the power supply and all capacitors in the circuit in figure gives the ac equivalent circuit in figure. If R_L is present, as shown, it appears in parallel with R_C in the ac equivalent circuit of AC Load Line of BJT.



(a) Circuit with coupling and bypass capacitors

(b) Power supply and capacitors behave as *ac* short-circuits

Figure
Voltage divider bias circuit with coupling and bypass capacitors, and the ac equivalent circuit

Once the ac equivalent circuit is drawn, the circuit ac performance can be investigated by drawing an AC Load Line of BJT, and by substituting a transistor model in place of the device.

The dc load for the circuit in Fig. 6-6(a) is ($R_C + R_E$), consequently, the dc load line is drawn for a total resistance of ($R_C + R_E$). Because the emitter resistor is capacitor bypassed in above figure (a), resistor R_E is not part of the circuit ac load. If external load R_L were not present, the circuit ac load would simply be R_C. With R_L capacitor-coupled to the circuit output, the ac load is $R_C||R_L$. An AC Load Line of BJT may now be drawn to represent the circuit ac performance.

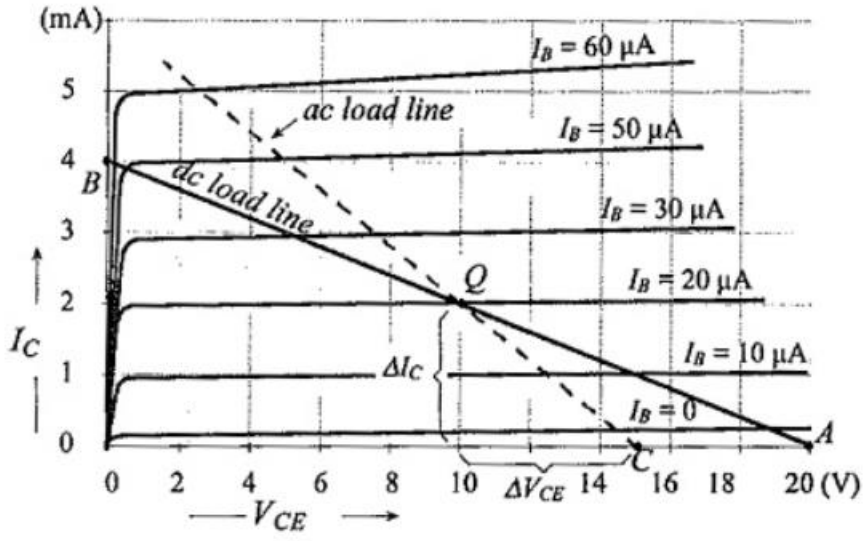


Figure
The ac load line for a transistor circuit is drawn through the Q-point.

When there is no input signal, the transistor voltage and current conditions are exactly indicated by the Q-point on the dc load line. An ac signal causes the transistor voltage and current levels to vary above and below the Q-point. Therefore, the Q-point is common to both the ac and dc load lines. Starting from the Q-point, another point is found on the AC Load Line of BJT by taking a convenient collector current change (usually $\Delta I_C = I_{CQ}$) and calculating the corresponding collector-emitter voltage change (ΔV_{CE}) as shown in the above figure.

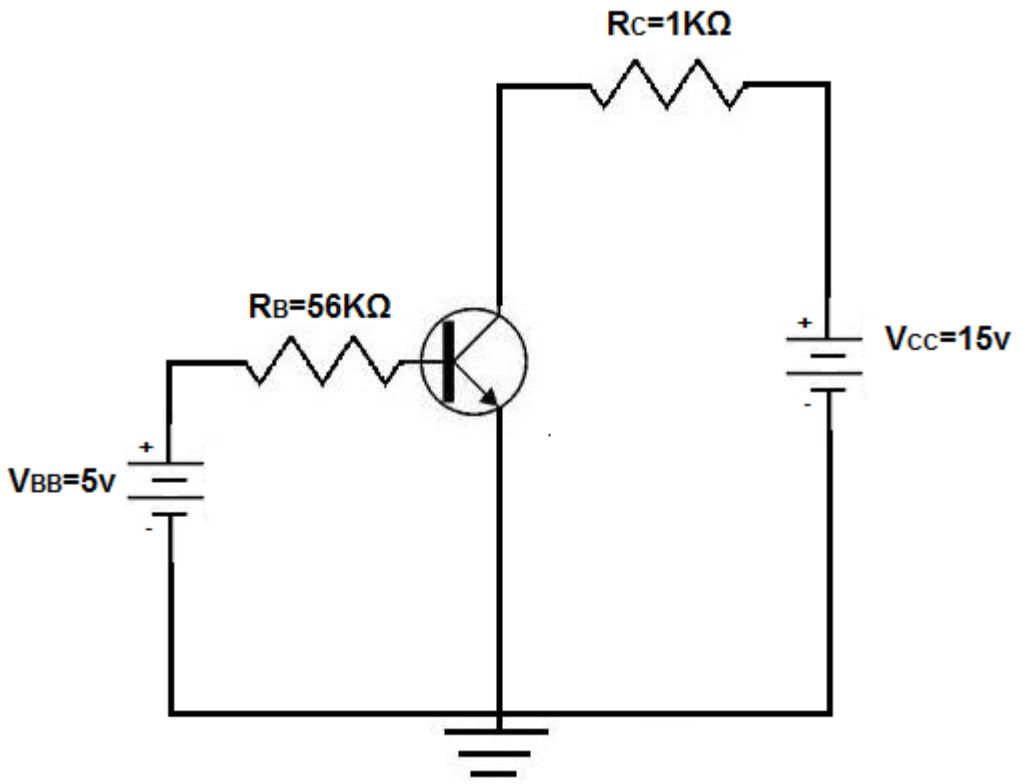
Transistor Biasing Methods

In this article, we will go over the different ways in which a bipolar junction transistor (BJT) can be biased so that it can produce a stable and accurate output signal.
Transistor biasing is the controlled amount of voltage and current that must be given to a transistor for it to produce the desired amplification or switching effect.
In other words, transistors must be fed the correct or appropriate levels of voltages and/or currents to their various regions in order to function properly and amplify signals to the correct level. This controlled amount of voltage and/or currents fed to the different junctions of a transistor is transistor biasing.

Without appropriate transistor biasing, the transistor may not function at all or amplify very poorly, such as produce clipping of the signal or produce too low of gain. Therefore, it's very important that a transistor is biased correctly for it to produce the intended output effect.

Base Bias

Base bias the simplest way to bias a BJT transistor. Base bias ensures that the voltage fed to the base, VBB, is the correct voltage, which then supplies the correct current so that the BJT has enough base current to switch the transistor ON, below is a typical BJT receiving base bias:



VBB is the base supply voltage, which is used to give the transistor sufficient current to turn the transistor on. RB is a resistance value that is used to provide the desired value of base current I B. VCC is the collector supply voltage, which is required for a transistor to have sufficient power to operate. This voltage, reverse-biases the transistor, so that the transistor has sufficient power to have an amplified output collector current. The collector resistor, RC provides the desired voltage in the collector circuit.
Using the base biasing method, the collector current IC is dependent only on the values of βdc and IB. βdc is the amplification factor by which the base current gets amplified by. So the total output current, IC will be IC=βdc x IB.

Base Bias Voltage/Current Calculations

When using any biasing technique, calculations must be made of the various voltages and currents through a BJT transistor. Or else, it's impossible to tell whether the voltage and current values are correct or not.
The first calculation we will make is for the base current IB.
The base current can be found by dividing the voltage across resistor RB by the value of RB

IB= (VBB - VBE)/RB

Since the voltage drop across a silicon junction is 0.7V, the value of VBE=0.7V. Therefore, IB equals:

IB= (VBB - VBE)/RB= (5v - 0.7v)/56kΩ= 76.78µA

IC is calculated as:

$$\mathbf{IC=\beta dc \times IB= 100 \times 76.78\mu A \approx 7.68mA}$$

With IC then known, the collector-emitter voltage, VCE can be calculated. This is shown below:

$$\mathbf{VCE= VCC - IC \times RC= 15v - (7.68mA \times 1K\Omega)= 7.32v}$$

Base bias can also be done with a single supply voltage, VCC, with VBB omitted. So instead of using VBB in calculations, you would just use VCC instead. The result of the calculations are still Same.

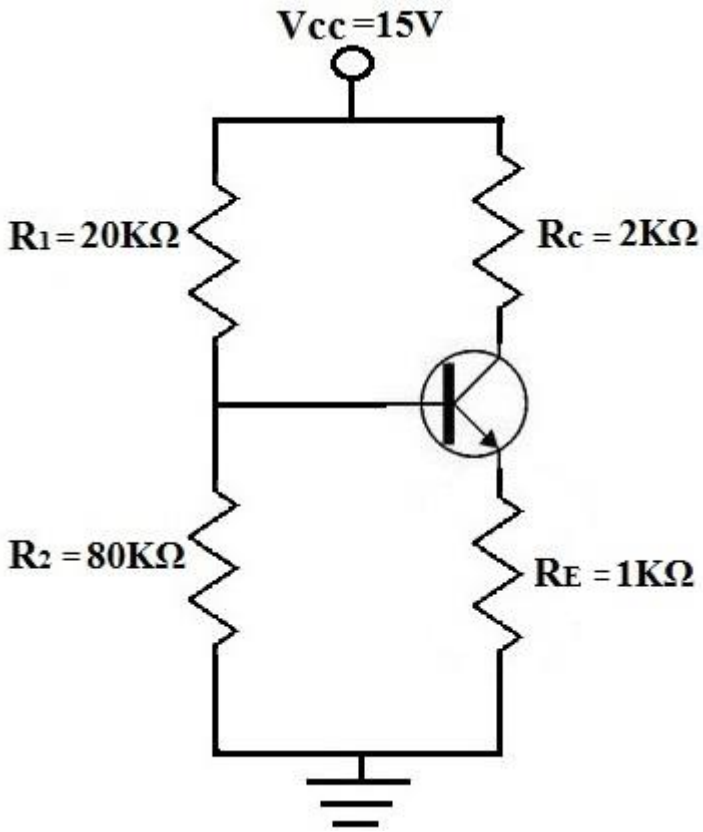
Disadvantages of Base Bias Method

Though base bias is one of the simplest and easiest methods to bias transistors, it is the least popular way to do so. This is because the collector current, IC, is decided by purely by the βdc of the transistor. βdc of a transistor is one of the most unstable and unpredictable parameters of a transistor. βdc can vary largely across transistors even of the same exact model and type. Therefore, base bias can lead to unpredictable actions if a transistor needs to be replaced and there are variations in the βdc of that transistor. βdc is also susceptible to changes due to temperature, as it can vary pretty largely due to ambient temperature. Base bias, then, can produce erratic circuit behavior due to transistor variations. Therefore, transistors are not commonly biased in this way.

We will explore other methods of transistor biasing including voltage-divider bias and emitter-supply bias, which provide more stability against the changes that may exist in β of a transistor.

Voltage Divider Bias

Another way to bias a transistor is by voltage divider bias.
Voltage divider bias is the most popular and used way to bias a transistor. It uses a few resistors to make sure that voltage is divided and distributed into the transistor at correct levels. One resistor, the emitter resistor, RE also helps provide stability against variations in β that may exist from transistor to transistor. BJT receiving voltage divider bias is shown below:



For the circuit above, we're going to assume that β=100 for the transistor. The base supply voltage, VBB, is calculated by:

$$V_{BB} = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right)$$

We Calculate RB below, which we will use the next calculation for IE.

$$R_B = R_1 \parallel R_2$$

$$= 10K\Omega \frac{(20K\Omega)}{(100K\Omega)} = 16K\Omega$$

Then, we calculate for the emitter current using the following formula:

$$I_{EQ} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{(\beta+1)} + R_E} = \frac{12V - 0.7V}{\frac{16K\Omega}{100} + 1K\Omega} = 9.74ma$$

The collector current IC is approximately equal to the emitter current.
IC≈ IE

How Emitter Resistor, RE, Fights Against the Instability of β

The RE provides stability in gain of the emitter current of a transistor circuit. of a transistor, its gain or amplification factor, can vary by large amounts from transistor to transistor, even if they're the same exact type from the same batch. There is no way to replicate the same exact βs across transistors. Therefore, when we are designing transistor circuits where we want roughly the same gain in all of them, we must design them in a way that produces the same gain despite fluctuations in the β values. We do this by carefully choosing the emitter resistance, RE, which provides stability against differences in β. RE provides stability in gain of the output current of a transistor circuit.

Resistor, R_E, fights against the instability of β

$$I_{EQ} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{(\beta+1)} + R_E}$$

Since R_E is usually much larger than $\frac{R_B}{(\beta+1)}$, it is the dominating factor of the denominator. So even though β may fluctuate widely between transistors, R_E's much larger value essentially overrides it and allows for stability against these fluctuations.

For the above transistor, the β was equal to 100. But let's say we have to swamp out that transistor and the new transistor has a β of 150. What will the new calculation be, and will the output current of the transistor swing largely in changes to the β or will it vary little and still be stable?

$$I_{EQ} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{(\beta+1)} + R_E} = \frac{12V - 0.7V}{\frac{16K\Omega}{150} + 1K\Omega} = 10.21ma$$

The answer is, the transistor output current doesn't vary much despite the large difference in β values of the transistors. Even though there is a difference of 50 of β in the transistors, there is less than a half of milliampere difference in the output current, IE. If wanted, an even larger value of

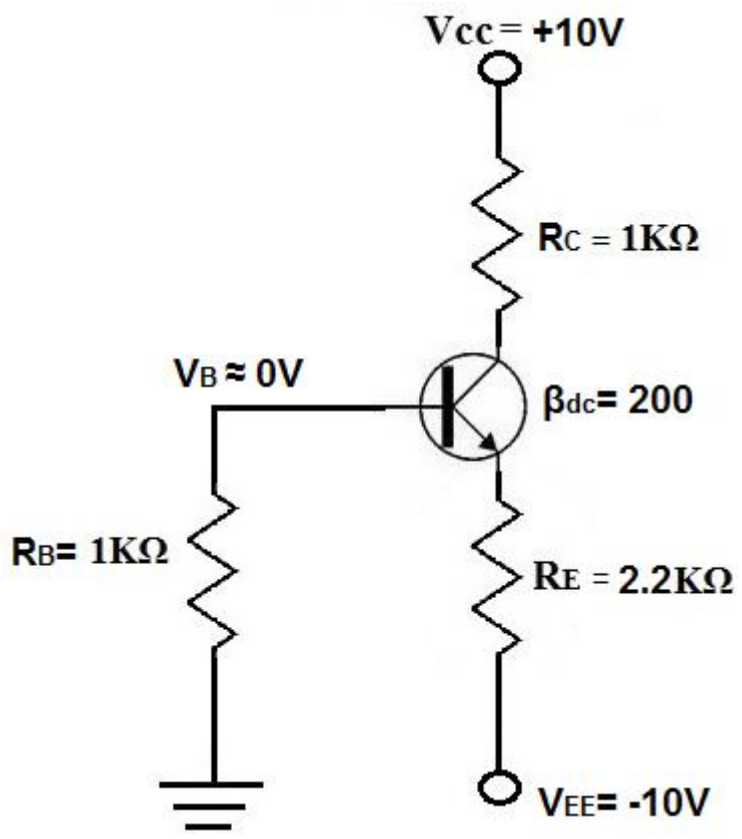
RE can be used so that there is even more stability against the β of transistors. However, realize that the larger RE is, the more gain that is lost for amplification in the circuit. So there must be balance in the design of the value of RE.

Advantages of the Voltage Divider Bias

Again, voltage divider bias is the most popular and used way to bias BJT transistors. The resistors help to give complete control over the voltage and current that each region receives in the transistor. And the emitter resistor, RE, allows for stability of the gain of the transistor, despite flucations in the β Values.

Emitter Bias

Another way to bias a transistor is emitter bias.
Emitter bias is a very good and stable way to bias transistors if both positive and negative power supplies are available. Emitter bias fluctuates very little with temperature variation and transistor replacement.
Below is a BJT transistor receiving emitter bias:



You can see how that both positive and negative voltage supplies are necessary to bias a transistor in this way. Positive voltage is fed to the collector of the transistor and negative voltage is fed to the emitter.

Calculations
Assuming this is a silicon transistor, the voltage drop across the base-emitter diode is equal to 0.7V.

To calculate the emitter current, IE, the formula is:

$$I_{EQ} = \frac{V_{EE} - V_{BE}}{\frac{R_B}{(\beta_{dc})} + R_E}$$

So, in the circuit above, the emitter current calculation is:

IE= (10V - 0.7V)/(2.2KΩ + (1KΩ/200))= 4.22mA

To calculate the collector voltage, VC, the formula is:

VC= VCC - ICRC = 10V - (4.23mA x 1KΩ) =5.77V

Again, emitter bias is an effective way to bias a BJT transistor. However, the voltage divider bias is still the most popular way to do so, while base bias is the least popular way because of the instability it provides if β changes.

Stabilization

The process of making the operating point independent of temperature changes or variations in transistor parameters is known as Stabilization.

Once the stabilization is achieved, the values of IC and VCE become independent of temperature variations or replacement of transistor. A good biasing circuit helps in the stabilization of operating point.

Need for Stabilization!

Stabilization of the operating point has to be achieved due to the following reasons.

- Temperature dependence of I_C
- Individual variations
- Thermal runaway

Let us understand these concepts in detail.

Temperature Dependence of I_C

As the expression for collector current IC is

$$IC=\beta I_B+I_{CEO} = \beta I_B+(\beta+1)\ I_{CBO}$$

The collector leakage current ICBO is greatly influenced by temperature variations. To come out of this, the biasing conditions are set so that zero signal collector current IC = 1 mA. Therefore, the operating point needs to be stabilized i.e. it is necessary to keep IC constant.

Individual Variations

As the value of β and the value of V_{BE} are not same for every transistor, whenever a transistor is replaced, the operating point tends to change. Hence it is necessary to stabilize the operating point.

Thermal Runaway

As the expression for collector current I_C is

$$IC=\beta I_B+I_{CEO} = \beta I_B+(\beta+1)\ I_{CBO}$$

The flow of collector current and the collector leakage current causes heat dissipation. If the operating point is not stabilized, there occurs a cumulative effect which increases this heat dissipation.

The self-destruction of such an un-stabilized transistor is known as **Thermal run away**.
In order to avoid **thermal runaway** and the destruction of transistor, it is necessary to stabilize the operating point, i.e., to keep I_C constant.

Stability Factor

It is understood that IC should be kept constant in spite of variations of ICBO or ICO. The extent to which a biasing circuit is successful in maintaining this is measured by Stability factor. It denoted by S.

By definition, the rate of change of collector current IC with respect to the collector leakage current ICO at constant β and IB is called Stability factor.

$$S = \frac{dI_C}{dI_{CO}} \quad \text{at constant } I_B \text{ and } \beta$$

Hence we can understand that any change in collector leakage current changes the collector current to a great extent. The stability factor should be as low as possible so that the collector current doesn't get affected. S=1 is the ideal value.

The general expression of stability factor for a CE configuration can be obtained as under.

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

Differentiating above expression with respect to I_C, we get

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

OR

$$1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S}$$

Since $\frac{dI_{CO}}{dI_C} = \frac{1}{S}$

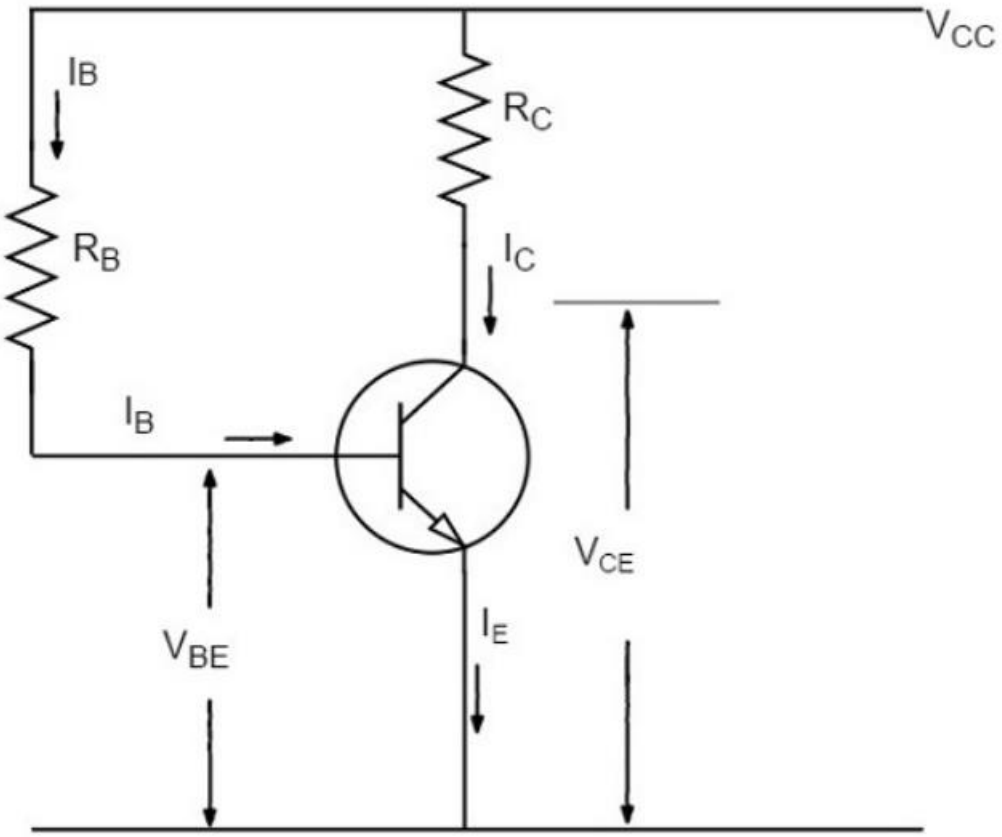
$$S = \frac{\beta + 1}{1 - \beta \left(\frac{dI_B}{dI_C} \right)}$$

Hence the stability factor S depends on β, I_B and I_C.

Fixed Bias

In this method, a resistor RB of high resistance is connected in base, as the name implies. The required zero signal base current is provided by VCC which flows through RB. The base emitter junction is forward biased, as base is positive with respect to emitter.

The required value of zero signal base current and hence the collector current (as IC = βIB) can be made to flow by selecting the proper value of base resistor RB. Hence the value of RB is to be known. The figure below shows how a base resistor method of biasing circuit looks like.



Let I_C be the required zero signal collector current. Therefore,

$$I_B = \frac{I_C}{\beta}$$

Considering the closed circuit from V_{CC}, base, emitter and ground, while applying the Kirchhoff's voltage law, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B R_B = V_{CC} - V_{BE}$$

Therefore,

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

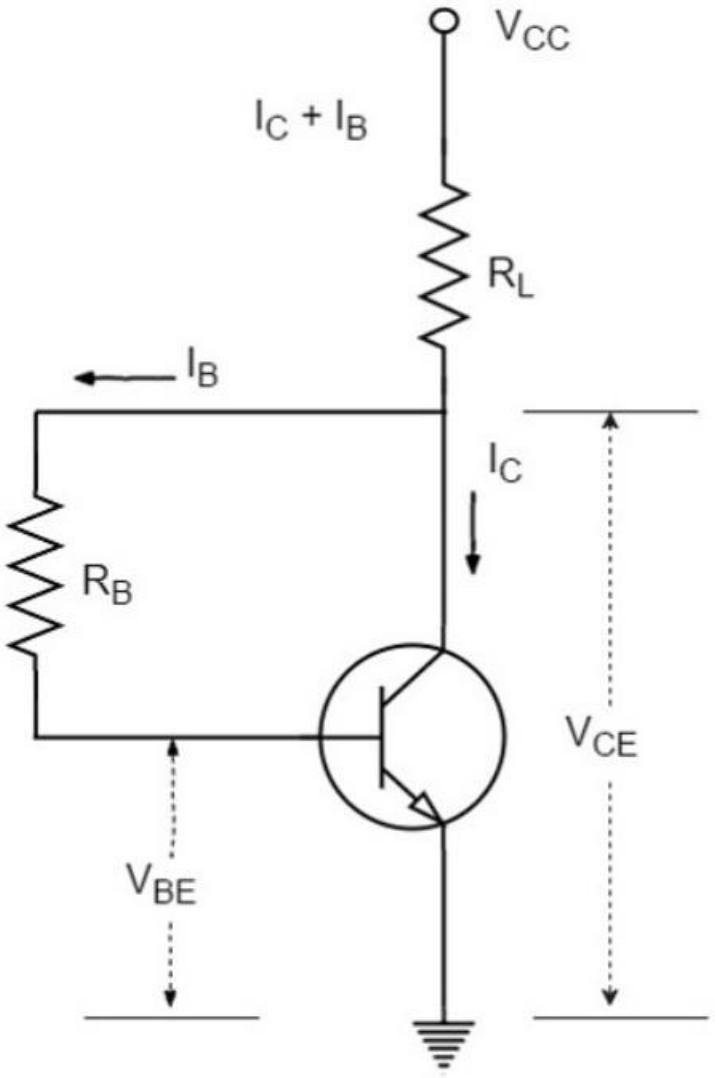
Since V_{BE} is generally quite small as compared to V_{CC}, the former can be neglected with little error. Then,

$$R_B = \frac{V_{CC}}{I_B}$$

We know that V_{CC} is a fixed known quantity and I_B is chosen at some suitable value. As R_B can be found directly, this method is called as **fixed bias method**.

Collector to Base Bias

The collector to base bias circuit is same as base bias circuit except that the base resistor R_B is returned to collector, rather than to V_{CC} supply as shown in the figure below.



This circuit helps in improving the stability considerably. If the value of IC increases, the voltage across RL increases and hence the VCE also increases. This in turn reduces the base current IB. This action somewhat compensates the original increase.

The required value of RB needed to give the zero-signal collector current IC can be calculated as follows.

Voltage drop across RL will be,

$$R_L = (I_C + I_B)R_L \cong I_C R_L$$

From the figure,

$$I_C R_L + I_B R_B + V_{BE} = V_{CC}$$

$$I_B R_B = V_{CC} - V_{BE} - I_C R_L$$

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_L}{I_B}$$

$$R_B = \frac{(V_{CC} - V_{BE} - I_C R_L)\beta}{I_C}$$

Applying KVL to the above equation

$$(I_B + I_C)R_L + I_B R_B + V_{BE} = V_{CC}$$

$$I_B(R_L + R_B) + I_C R_L + V_{BE} = V_{CC}$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_L}{R_L + R_B}$$

Since V_{BE} is almost independent of collector current, we get

$$\frac{dI_B}{dI_C} = -\frac{R_L}{R_L + R_B}$$

We know that,

$$S = \frac{1 + \beta}{1 - \beta(dI_B/dI_C)}$$

$$S = \frac{1 + \beta}{1 + \beta\left(\frac{R_L}{R_L + R_B}\right)}$$

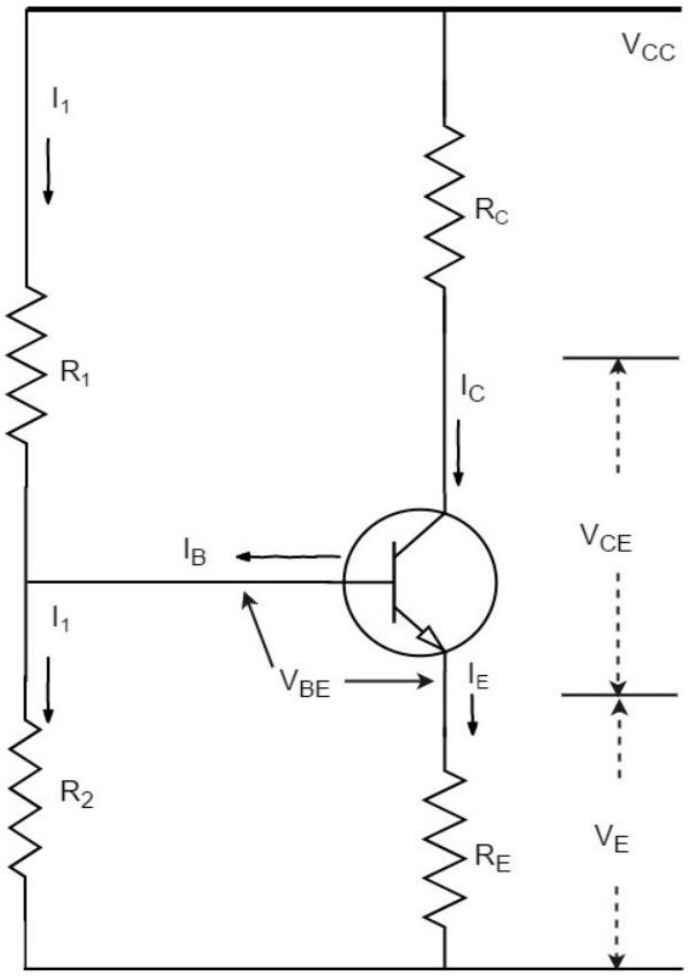
This value is smaller than (1+β) which is obtained for fixed bias circuit. Thus, there is an improvement in the stability.

This circuit provides a negative feedback which reduces the gain of the amplifier. So, the increased stability of the collector to base bias circuit is obtained at the cost of AC voltage gain.

Self-Biasing or Voltage Divide Bias

Among all the methods of providing biasing and stabilization, the voltage divider bias method is the most prominent one. Here, two resistors R1 and R2 are employed, which are connected to VCC and provide biasing. The resistor RE employed in the emitter provides stabilization.

The name voltage divider comes from the voltage divider formed by R1 and R2. The voltage drop across R2 forward biases the base-emitter junction. This causes the base current and hence collector current flow in the zero signal conditions. The figure below shows the circuit of voltage divider bias method.



Suppose that the current flowing through resistance R1 is I1. As base current I_B is very small, therefore, it can be assumed with reasonable accuracy that current flowing through R2 is also I1.

Now let us try to derive the expressions for collector current and collector voltage.

Collector Current, I_C
From the circuit, it is evident that,

$$I1 = V_{CC}R1 + R2$$

Therefore, the voltage across resistance R2 is,

$$V2 = (V_{CC}R1 + R2)\ R2$$

Applying Kirchhoff's voltage law to the base circuit,

$$V2 = V_{BE} + V_E$$

$$V2 = V_{BE} + I_E R_E$$

$$I_E = V2 - V_{BE}R_E$$

Since IE ≈ IC,

$$I_C = V2 - V_{BE}R_E$$

From the above expression, it is evident that I_C does not depend upon β. V_{BE} is very small that I_C does not get affected by V_{BE} at all. Thus, I_C in this circuit is almost independent of transistor parameters and hence good stabilization is achieved.

Collector-Emitter Voltage, VCE

Applying Kirchhoff's voltage law to the collector side,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

Since IE ≅ IC

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CC} = I_C\ (R_C + R_E) + VCE$$

Therefore,

$$V_{CE} = V_{CC} - I_C\ (R_C + R_E)$$

R_E provides excellent stabilization in this circuit.

$$V2 = V_{BE} + I_C R_E$$

Suppose there is a rise in temperature, then the collector current I_C decreases, which causes the voltage drop across R_E to increase. As the voltage drop across R2 is V2, which is independent of IC, the value of V_{BE} decreases. The reduced value of I_B tends to restore I_C to the original value.

Chapter-VI

Junction Field Effect Transistor

Junction Field Effect Transistor

Introduction to J-FET, Types of J-FET, V-I Characteristics of J-FET in CS configuration, FET as an amplifier, J-FET Biasing.

6.0 OBJECTIVES

After completion of this chapter we should be able to understand :

- To know the principle of operation of JFET and MOSFET.
- To learn the analysis of field effect transistor using parameters.
- To know the various biasing methods on field effect transistor.
- Characteristics of field effect transistors in different configurations.

6.1 INTRODUCTION

The Field-effect transistor amplifiers provide an excellent voltage gain with an added feature of high input impedance. They are also low-power-consumption configurations with good frequency range and minimal size and weight.

The FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. FET is a voltage-controlled device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. The FET can be used as a linear amplifier or as a digital device in logic circuits. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications.

6.2 FET (FIELD EFFECT TRANSISTOR)

Field Effect Transistor: This is a semiconductor device in which the output current is controlled by the applied electric field. The current in a FET is carried only by one type of majority charge carriers-electrons (or) holes. It is also called as *unipolar transistor*.

The FETs are unipolar devices because they operate only with one type of charge carrier. If the channel conduction and hence the current in the device from source to drain can be controlled by the application of an electric potential or transverse electric field introduced by gate, the device is known as Field effect transistor (FET).

The term field effect stands for the fact that the operation of the device mainly depends on the electric field applied between its terminals called Gate and source analogous to the base and collector in transistor to control the current through it. The major feature of FETs is their high input resistance.

The field effect transistor is available in several forms. Two most important forms are,

1. Junction field effect transistor (JFET)
2. Insulated gate field effect transistor (IGFET) or metal oxide semiconductor field effect transistor (MOSFET) or (MOST).

6.2.1 Comparison of FET over BJT

FET	BJT
The relationship between input and output quantities in non-linear due to square term in shockley's equation is, $I_D = T_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$	The BJT is an almost linear device or BJT works linearly in active region as an amplifier.
FET's are named as source, drain and gate.	The BJT is three terminals can be named as the base, emitter and collector.
The Higher frequency response.	Frequency variation affects the performance.
FET is an Unipolar semiconductor device because of its operation can be depends upon the flow of majority carriers i.e., either holes or electrons as the case may be.	The BJT is a bipolar semiconductor device because the current constituting elements are both majority carriers.
The input impedance of FET is much more larger than BJT. The reason behind this is that an input terminal i.e., gate to source of FET can be reverse biased and reverse bias offers ideally infinite resistance.	The input impedance of BJT is very less in comparison to FET.
It is costlier than BJT	It is relatively cheaper
It have good thermal stability because of absence of minority carriers.	These are temperature dependent, thermal runaway may cause.
FET is a voltage controlled device	BJT is a current controlled device
Small gain bandwidth product	Greater than FET
Small sized	Comparatively bigger

6.2.2 Classification of FET

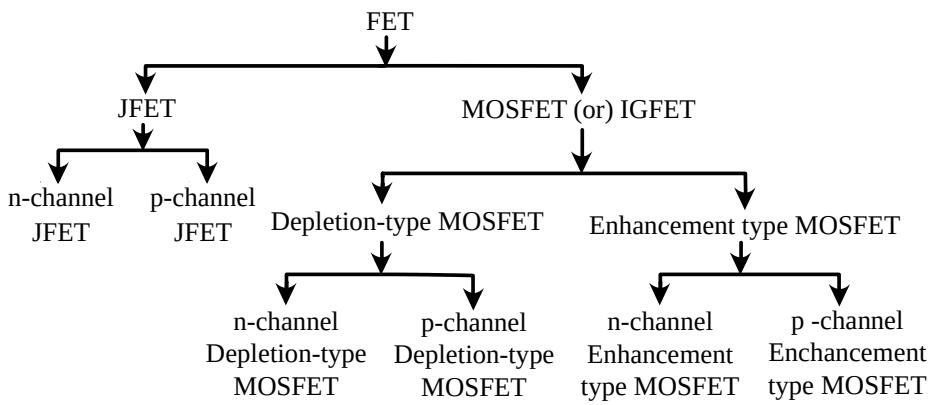


Figure 6.1: Different types of field effect transistors

6.3 JFET

Junction Field Effect Transistor (JUGFET or JFET) has no PN-junctions but instead has a narrow piece of high-resistivity semiconductor material forming the "Channel" of either N-type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly is called the Drain and Source respectively.

Based on the majority carriers, JFET has been classified into two types, namely,

1. N-Channel JFET with electrons as the majority carriers, and
2. P-Channel JFET with holes as the majority carriers.

Likewise, the P-channel JFET's channel can be doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types. Since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET's a more efficient conductor compared to their P-channel counterparts.

Symbols: JFET is a unipolar-transistor, which acts as a voltage controlled current device and is a device in which current at two electrodes is controlled by the action of an electric field at a p-n junction. It consists of three terminals like Gate (G), Drain (D) and Source (S).

In these 3 terminals, the Gate terminal acts as a controlling terminal. BJT acts as a current controlling device. FET also acts as a voltage controlling device. Here, the voltage between gate and source controls the drain current. Hence, it is called as voltage controlled device.

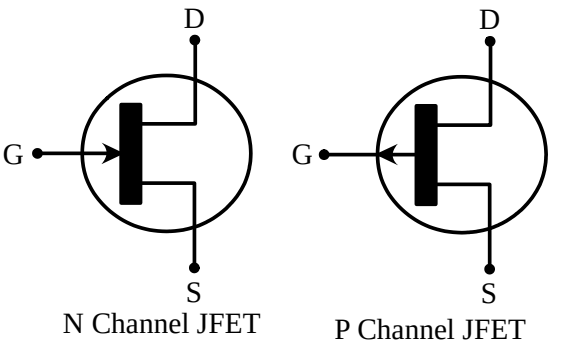


Figure 6.2: Symbols of JFET

6.3.1 Construction of JFET

The junction field effect transistor is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons and holes. JFET consists of p-type or n-type silicon material containing two pn junction at the sides.

If the bar is n-type is called as n-channel JFET and when the bar is p-type is called as p-channel JFET. The two pn junctions forming diodes can be connected internally and common terminal is called as gate is taken out. Other terminals are source and drain.

P-channel JFET: P-channel JFET consists of p-type silicon bar forming a conducting channel for the charge carriers. The heavily doped n-regions introduced on both sides of bar form the gate. It can be used to control the flow of holes from source to drain. Construction of JFET as shown in figure 6.3.

N-channel JFET: N-channel JFET consists of n-type silicon bar foaming the conducting channel for the charge carriers. The heavily doped p-regions introduced on both sides of the bar form the gate. It can be used to control the flow of electrons from source to drain.

- **Source:** This terminal is connected to the negative pole of the battery. Electrons which are the majority carriers in the N- type bar enter the bar through this terminal.
- **Drain:** This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.
- **Gate:** Heavily doped p- type silicon is diffused on both sides of the N- type silicon bar by which PN- junction are forced. These layers, are joined together and called gate G..
- **Channel:** The region BC of the N- type bar between the depletion region is called the channel. Majority carriers move from the source to drain when a potential difference V_{DS} is applied b/w the source & drain.

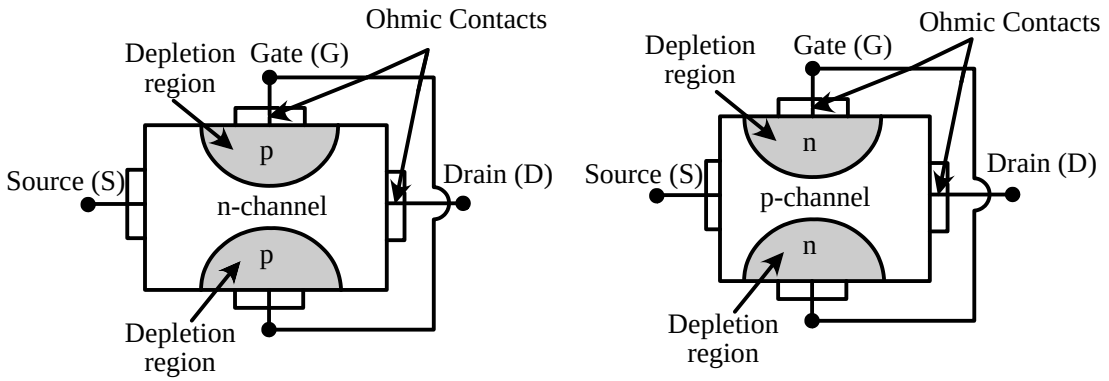


Figure 6.3: JFET Construction

6.3.2 JFET Polarities

Figure 6.4 (a) shows the n-channel JFET polarities whereas figure 6.4 (b) shows p-channel JFET polarities. In each case, the voltage between the gate and source is such that the gate can be reverse biased. This is the normal way of JFET connection. The drain and sources are interchangeable i.e., either end can be used as source and an other end as drain.

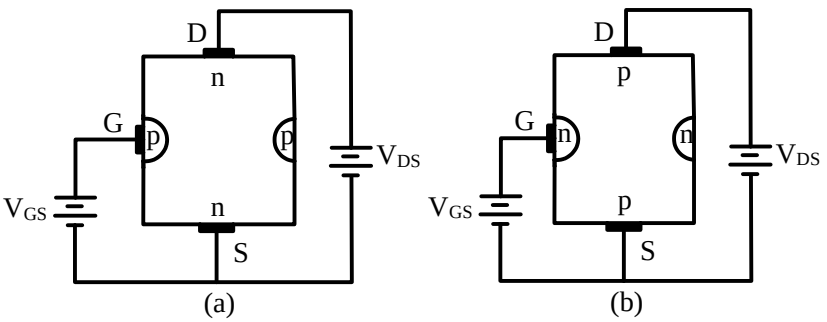


Figure 6.4: JFET polarities

6.3.3 Operation and Working of JFET

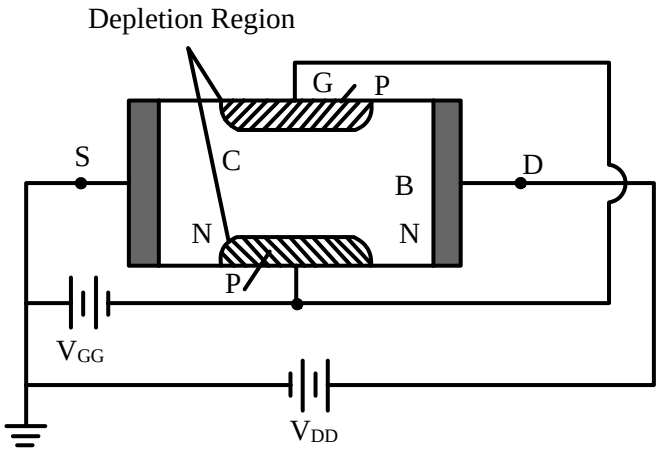


Figure 6.5: JFET operation

To consider the operation of a JFET as shown in figure 6.6. The application of voltage $V_{DS} = V_{DD}$ drain supply voltage from drain to source will cause the electrons to flow through the channel. The amount of drain current I_D can be initially determined by the value of V_{DS} since it is just the ohmic resistance of bar from S to D i.e., limiting the current.

In order to see what effect will be a voltage V_{GS} from gate to source, have on this drain current for a given drain to source voltage, if the P-N junctions between gate and source are under reverse-bias conditions. These reverse biased P-N junctions can develop depletion regions as shown by cross-hatching in figure 6.4.

The depletion regions are non-conductive except for a few intrinsic carriers and decrease the conductance of channel between source and drain electrodes. If the reverse bias is increased, the size of the depletion regions increases and drain current can bereduced.

If the reverse current is large enough for two depletion regions to meet the channel becomes pinched off and drain current cuts-off. The reverse bias can be required for pinch off is labelled as V_P. The drain current through the channel depends upon the degree to which the electric field (due to the change in the depletion region) extends into channel and provides the effect of decreasing the conductance through an transistor. Thus, the name field-effect transistor (FET) given to this device.

In a bar of P-type semiconductor, the gate is formed due to N-type semiconductor. Working of the P-channel JFET will be similar to that of N-channel JFET with the proper alterations in the biasing circuits. In this case holes will be the current carriers instead of electrons.

The circuit symbols for N-channel and P-channel JFETs are shown in figure 6.6. It should be noted that the direction of arrow points in the direction of conventional current which would flow into gate if the PN junction was forward biased.

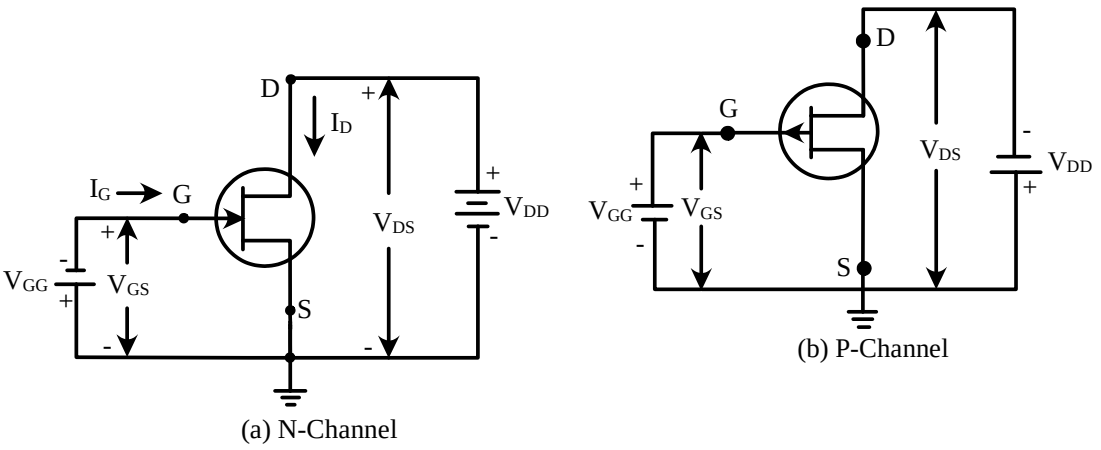


Figure 6.6: N-channel JFET

6.3.4 Drain Current

To find an expression for drain current, the current in the channel resistance is proportional to V_{DS} in accordance with the Ohm's law, and to $V_{GS} - V_P$ because of pinch off. The finite drain voltage also results in an additional reverse bias varying from zero at source end to V_{DS} at the drain end. The average reverse bias can be taken as $\frac{V_{DS}}{2}$. The drain current is,

$$I_D = K\left[V_{GS} - V_P - \left(\frac{V_{DS}}{2}\right)\right]V_{DS}$$

Where K is the constant.

At pinch off, the sum of gate voltage and drain voltage is $V_{GS} + V_{DS} = V_P$, so that the above equation becomes,

$$I_D = K\left[V_{GS} - V_P - \left(\frac{V_{GS} - V_P}{2}\right)\right](V_{GS} - V_P) = \frac{K}{2}(V_{GS} - V_P)^2$$

6.4 WORKING OPERATION OF N-CHANNEL JFET

Case (i): When $V_{GS} = 0$ and $V_{DS} = 0$

If no voltage is applied between drain and source, gate and source, the thickness of depletion regions round the P-N junction is uniform as shown in figure 6.7. Here, the drain current $I_D = 0$ if $V_{DS} = 0$. The depletion region around the P_D junctions are of equal thickmess and symmetrical.

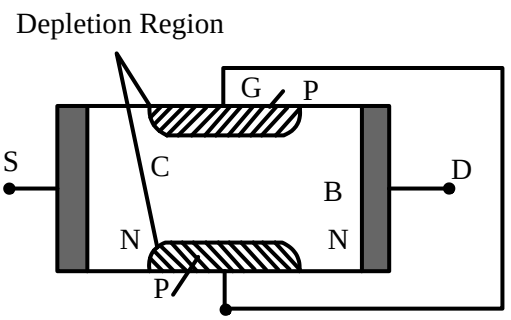


Figure 6.7: Thickness of the depletion regions

Case (ii): When $V_{DS} = 0$ and V_{GS} is decreased

The P-N junctions are reverse-biased and hence the thickness of depletion region can be increases. If V_{GS} is decreased from zero, the gate reverse bias increases. Thickness of the depletion region in the channel increases until the two depletion regions make contact with an each other. In this condition, the channel is said to be cut-off and gain current becomes zero. Value of V_{GS} which is required to cut-off the channel is called cut-off voltage V_C.

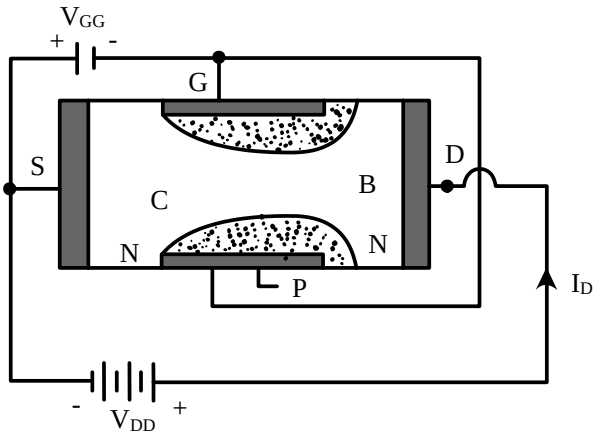


Figure 6.8: JFET under Applied Bias

Case (iii): When $V_{GS} = 0$ and V_{DS} is increased from Zero

In this case the drain is positive with respect to the source. Now the majority carriers (electrons) flows through the N-Channel from source to drain. Thus, the conventional current I_D flows from drain to source. The magnitude of the current can be depends upon the following factors:

1. Conductivity of channel
2. Length of channel
3. Cross-sectional area 'A' of channel.
4. Magnitude of applied voltage V_{DS}.

The channel acts as a resistor of resistance 'R' is,

$$I_D = \frac{V_{DS}}{R} = \frac{AV_{DS}}{\rho L}$$

Where ' ρ ' is the resistivity of channel.

6.5 DRAIN AND TRANSFER CHARACTERISTICS OF JFET

Drain Characteristics of JFET: If V_{DS} increases, the reverse voltage across the P-N junction increase and hence the thickness of depletion region can also increases. Hence, the channel is wedge shaped as shown in figure 6.8. If V_{DS} increases at a certain value V_P of V_{DS}, the cross sectional area of channel becomes minimum. At this voltage, an channel is said to be pinched off and drain voltage V_P is called as pinch-off voltage. Decreasing cross-section of channel with an increase of V_{DS} then following results can be obtained.

a) If V_{DS} is increased from zero, I_D increases linearly along OP, this region from $V_{DS} = 0$ to $V_{DS} = V_P$ is called as an ohmic region. In this region, the FET acts as a voltage variable resistor (VVR) or the voltage dependent resistor (VDR).

b) If $V_{DS} = V_P$, I_D becomes maximum. When V_{DS} increased beyond V_P, the length of pinch-off (or) saturation region increases. Thus, there is no further increase of I_D.

c) At a certain voltage corresponding to the point B, I_D suddenly increases. Due to this effect is the Avalanche multiplication of electrons can be caused by breaking of the covalent bonds of silicon atoms in the depletion region between gate and drain. Drain voltage at which the breakdown can be occurs is denoted by BV_{DGO}.

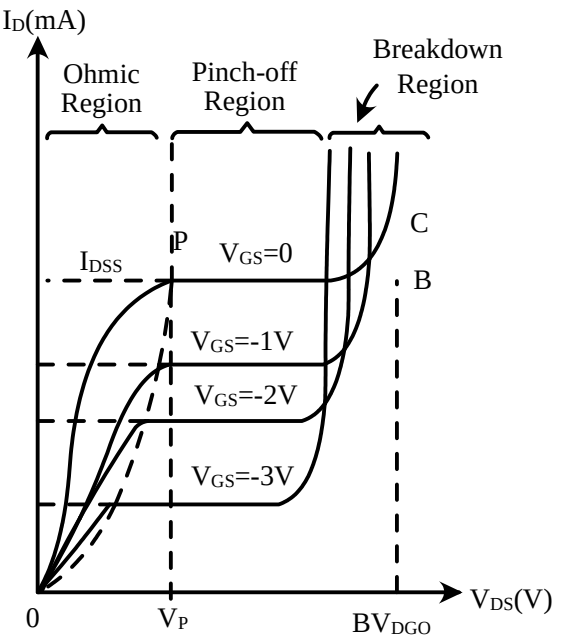


Figure 6.9: Characteristics of n-channel JFET

iv) When V_{GS} is negative and V_{DS} is increased: If the gate can be maintained at a negative voltage less than negative cut-off voltage, the reverse voltage across the junction is further increased. Since for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for $V_{GS} = 0$, but the values of V_P and BV_{DGO} are lower.

Drain current I_D can be controlled by the electric field that extends into the channel due to reverse biased voltage applied to gate. Thus, this device has been given the name Field Effect Transistor.

Region of Operation: $V_{DS} < V_P$

i. In this region $I_D \propto V_{DS}$ that is the property of a resistance. So this region in which JFET behaves as a resistance and follows the ohms law called as ohmic region.

ii. When $V_{DS} > V_P$, it acts as constant current source and it is also known as linear or saturation region.

iii. At $V_{GS} > -V_P$ ideally $I_D = 0$, devices turns off and it is called as cut-off region.

iv. At very high value of V_{DS}, breakdown occurs. This maximum value of V_{DSmax} can be specified on the FET data -sheet.

Transfer Characteristics of N-type JFET

To explain the basic operation of N-type JFET we have drawn the graph between drain current I_D and drain to source voltage V_{DS} taking gate to source voltage V_{GS} as a constant. It is called as drain characteristics or output characteristics. With the help of drain characteristics, we can

also find the characteristics showing the relation between drain current and gate to source (V_{GS}) voltage taking (V_{DS}) as constant. It is called transfer characteristics of JFET. A graph of the drain current as a function of the gate voltage (V_{GS}) is called the transconductance curve.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \Rightarrow \left(1-\frac{V_{GS}}{V_P}\right)^2 = \frac{I_D}{I_{DSS}}$$

$$1-\frac{V_{GS}}{V_p} = \sqrt{\frac{I_D}{I_{DSS}}} \Rightarrow V_{GS} = V_P\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right)$$

By reading the values of I_D and V_{GS} from figure 6.10 of depletion region width and p channel FET and its characteristics one can plot the transconductance curve.

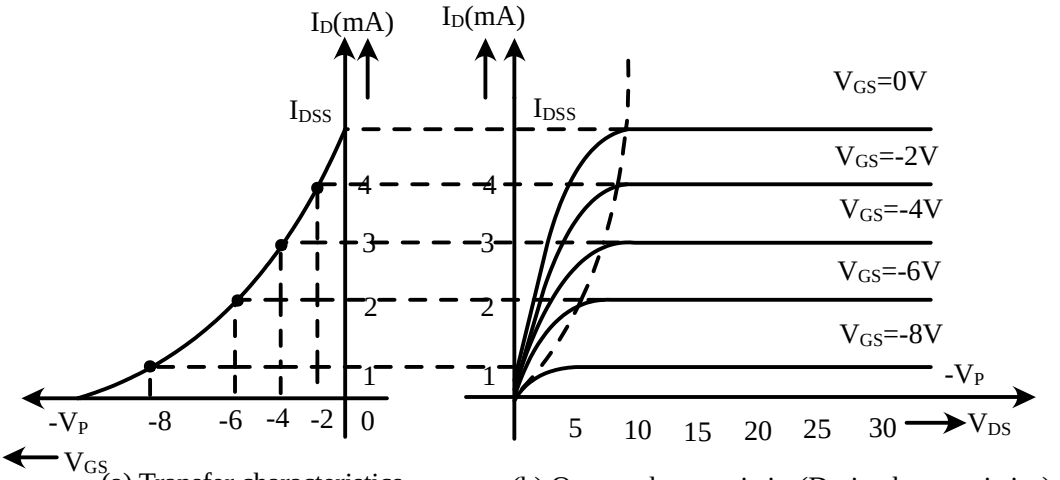


Figure 6.10: Characteristics of N-JFET

Here I_D is taken along y- axis & V_{GS} is taken along x - axis. When V_{GS} = 0V the drain current is maximum (I_{DSS}) when V_{GS} is increased (-ve side) then width of the decreases region increases. Therefore, the drain current diereses. At one particular voltage (V_{GS}), the channel width is said to be completely reduced and that voltage is called as pinch- off voltage. Here the drain current becomes equal to zero.

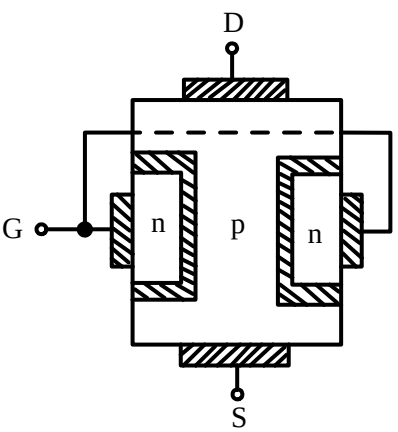
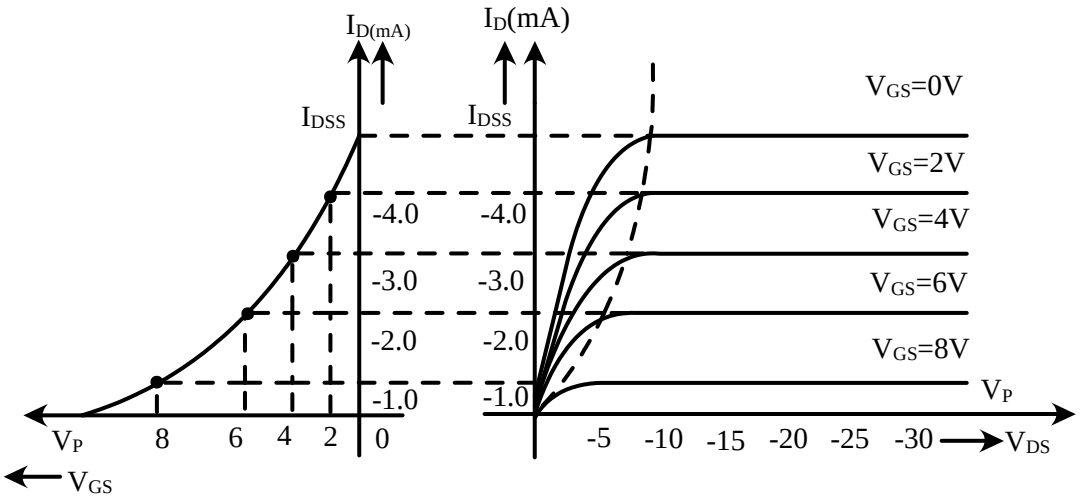


Figure 6.11: P-JFET

6.6 P-TYPE JFET

Only difference between P-type and N-type JFET is that P regions can be replaced by N-type and N regions can be replaced by P-type. Because of this, the polarities of volatges are changed.



(a) Transfer characteristics (b) Output characteristics (Drain characteristics)

Figure 6.12: Characteristics of P-JFET

Non-linear relation was proved by Shockley's equation. The Shockley equation is,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{... (1)}$$

Where I_{DSS} and V_P are constants for a particular device

V_P is the pinchoff voltage

The pinch-off voltage V_P is negative for the n-channel JFET and gate-to-source voltage is also negative. Therefore, the ratio $\frac{V_{GS}}{V_P}$ is positive.

Similarly, the pinch-off voltage for the p-channel JFET is positive and gate-to-source voltage V_{GS} is also positive. Thus, the ratio $\left(\frac{V_{GS}}{V_P}\right)$ is always positive.

For the n-channel device, the saturation region occurs when $V_{DS} \geq V_{DS(sat)}$

Where $V_{DS(sat)} = V_{GS} - V_P$ ... (2)

For the p-channel device, the saturation region occurs when $V_{SD} = V_P - V_{GS}$ ... (3)

6.7 DETERMINATION OF FET PARAMETERS

In a JFET, the drain current I_D depends upon the drain voltage V_{DS} and the gate voltage V_{GS}. Any one of these variables may be fixed and the relation between the other two is determined. These relations are determined by the three parameters which defined below.

1. Mutual Conductance (or) Transconductance g_m : It is the slope of the transfer characteristic curves. It can be defined as the ratio of change in drain current to the change in gate to source

voltage at constant drain-source voltage i.e.,

$$g_m = \frac{\text{Change in } I_D}{\text{Change in } V_{GS}}$$

When V_{DS} is constant

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}} \Big| V_{DS} \text{ is held constant} \quad \ldots (1)$$

Here it simplify the slope of transfer characteristics. Its unit is seimens (S) which was earlier called mho or A/V. It is also called transconductance (g_{fs}) or forward transmittance (Y_{fs}). The values range from 0.1 to 20mS for both JFETs and MOSFETs.

Shockley Equation: Mathematical Expression for $\mathbf{g_m}$

The Shockley equation is,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Where I_{DSS} = Drain saturation current

I_D = I_{DSS} when $V_{GS} = 0$

V_P = Pinch - off voltage

Differentiating both sides with respect to V_{GS}. We get,

$$\frac{dI_D}{dV_{GS}} = 2I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right)$$

$$g_m = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \ldots (2)$$

When $V_{GS} = 0$, $g_m = g_{m_0}$

$$g_{m_0} = -\frac{2I_{DSS}}{V_P} \quad \ldots (3)$$

From equation (2) and (3). We get,

$$g_m = g_{m_0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

2. A.C. Drain Resistance (r_d): This is the a.c. resistance between drain and source terminals when JFET operates in the pinch-off region. It can be defined as the ratio of the change in drain to source voltage to the change in drain current at constant gate source voltage. It is the reciprocal of the slope of the drain characteristics and is defined as,

$$r_d = \frac{\text{Change in } V_{DS}}{\text{Change in } I_D}$$

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \Big| V_{GS} \text{ is held constant}$$

The reciprocal of r_d is called as drain conductance. It can be denoted by g_d (or) g_m. The typical values of r_d range from $100k\Omega$ to $1m\Omega$ for a JFET and from $10k\Omega$ to $100k\Omega$ for a MOSFET.

3. D.C. Drain Resistance (R_{DS}): This is also called as the static or Ohmic resistance of the channel and is,

$$R_{DS} = \frac{V_{DS}}{I_D}$$

4. Amplification Factor μ: The two parameters g_m and r_d for JFET. It can be defined as the ratio of change in drain to source voltage to the change in gate to source voltage at constant drain current. The third parameter can be known as "amplification factor" is denoted by μ and is defined as,

$$\mu = \frac{\text{change in } V_{DS}}{\text{change in } V_{GS}}$$

$$\mu = -\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)_{I_D} = \frac{\Delta V_{DS}}{\Delta V_{GS}},\ I_D \text{ held constant.}$$

Thus, μ is the ratio of two voltages and it has no limits

For a JFET the value of μ is at the most 100.

Relationship among FET Parameters: As I_D on V_{DS} and V_{GS}, the functional equation can be expressed by,

$$I_D = f(V_{DS}, V_{GS})$$

When the drain voltage is changed by a small amount from V_{DS} to $(V_{DS} + \Delta V_{DS})$ and the gate voltage is changed by a small amount from V_{GS} to $(V_{GS} + \Delta V_{GS})$. The small change in ΔI_D is,

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS} \qquad \text{... (4)}$$

Dividing the both sides of equation (4) with ΔV_{GS},

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \cdot \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \cdot \left(\frac{\Delta V_{GS}}{\Delta V_{GS}}\right)$$

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

If I_D is constant, then $= \frac{\Delta I_D}{\Delta V_{GS}} = 0$

Hence, $0 = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \Rightarrow 0 = \left(\frac{1}{r_d}\right)(-\mu) + g_m$

Hence, $\mu = r_d x g_m \Rightarrow \mu = r_d g_m$

Thus, the parameter μ is the ratio of two similar quantities viz. ratio of two voltages μ is unitless.

Expression for Saturation Drain Current

$$I_{DS} = I_{D_{SS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Where I_{DS} = Saturation Drain Current

$I_{D_{SS}}$ = Value of I_{DS} when $V_{GS} = 0$

V_P = Pinch-off voltage

5. Input Resistance (R_i): The ratio of gate- source voltage to drain saturation current $R_i = \frac{V_{GS}}{I_{DSS}}$.

6. Power Decepation (P_d): Product of drain- source voltage and drain current $P_d = V_{DS} \times I_D$.

6.8 PINCH-OFF VOLTAGE

Pinch-off Voltage: Channel has Ohmic resistance and there is a potential difference V_{DS} between drain and source, there is a gradual increase in positive potential from source to drain. If the result of this reverse bias at the junctions and hence the width of depletion layers increases as we go from source to drain.

For this reason channel becomes wedge shaped with its narrow end near the drain. If V_{DS} is increased further, the width of channel becomes less and less till it is minimum and two depletion layers meet near the drain end. At this stage the channel is said to be pinched off. The value of V_{DS} at which pinch off takes place is called as pinch off voltage V_P.

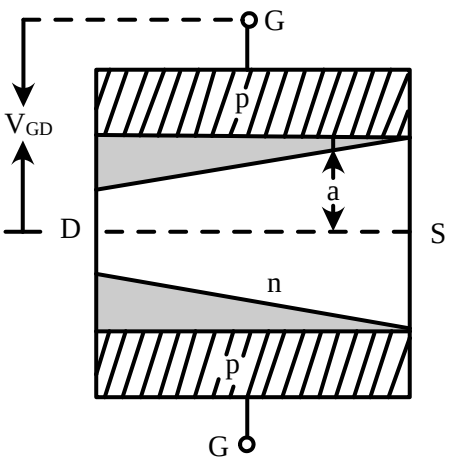


Figure 6.13

Expression for Pinch-off Voltage: Width of the depletion region for a PN junction to which a bias voltage V has been applied is,

$$W = \left[\frac{2\varepsilon}{e}(V_B - V)\left(\frac{1}{n_n} + \frac{1}{p_p}\right)\right]^{\frac{1}{2}} \quad \ldots (1)$$

But $n_n = N_d$, $p_p = N_a$

The equation (1) becomes,

$$W = \left[\frac{2\varepsilon_r\varepsilon_0}{e}\left(\frac{N_a + N_d}{N_a N_d}\right)(V_B - V)\right]^{\frac{1}{2}}$$

Where, V_B is contact potential.

N_a is concentration of acceptor ions (number of acceptor ions or $holes/cm^3 = p_p$) on p-side,

N_d concentration of donor ions (number of donor ions or $electrons/cm^3 = n_n$) on n-side.

e is the charge on electron (with negative sign).

ε_r is the relative permittivity of material and

ε_0 is the permittivity of free space.

Consider V_{GD} is the reverse bias between the gate and drain end of channel. It can be supposed that the gate region is being heavily doped. The depletion layer lies primarily in the n-type channel and its thickness within the p region is neglected. Due to the same reason $N_d << N_a$ and therefore N_d can be neglected as compared to N_a.

$$\frac{N_a + N_d}{N_a x N_d} = \frac{N_a}{N_a N_d} = \frac{1}{N_d}$$

It can be assumed that contact potential V_B is also negligible as compared to V_{GD}

$$V_B - V = -V_{GD}$$

W is the width of depletion layer at the drain end is,

$$W = \left[\frac{2\varepsilon_r \varepsilon_0}{e} \frac{(-V_{GD})}{N_d} \right]^{\frac{1}{2}}$$

The pinch-off occurs if the value of $-V_{GD} = V_p$ is such that width of depletion layer is equal to channel half width a Substituting $-V_{GD} = V_p$

$[\because$ pinch – off voltage is always a positive quantity$]$ and taking W=a. We get,

$$\frac{2\varepsilon_e \varepsilon_0}{e} \frac{V_p}{N_d} = a^2$$

$$V_P = \frac{ea^2 N_d}{2\varepsilon_r \varepsilon_0} = \frac{ea^2 N_d}{2\varepsilon}$$

For a p-type channel, the pinch off voltage $V_P = \frac{ea^2 N_a}{2\varepsilon}$

6.9 APPLICATION OF FET AS VOLTAGE VARIABLE RESISTOR

FET as a Voltage Variable Resistor (VVR)

In most linear applications of field effect transistors the device is operated in the constant current portion of its output characteristics. But some times FET can be operated in the region before pinch-off, where V_{DS} is small. In this region, the FET is useful as a voltage variable resistor i.e., the drain to source resistance is controlled by the bias voltage V_{GS}. In this region the FET is

called as voltage variable resistor (VVR). The variation of r_d with V_{GS} for 2N3277 can be plotted as shown in figure 6.14. The variation of r_d with V_{GS} can be given by the empirical expression is,

$$r_d = \frac{r_0}{1 - KV_{GS}}$$

Where, r_0 = Drain resistance at zero gate bias

K=Constant, dependent on FET type

V_{GS} = Gate to source voltage.

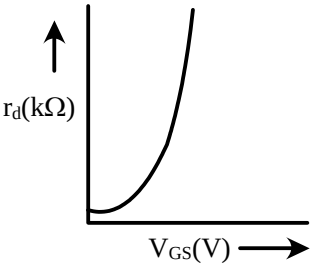


Figure 6.14

Thus, the FET can be operated in this region acts like a variable passive resistor, so it can be used to vary the voltage gain of a multi-stage amplifier A as the signal level is increased. This action is called as AGC (Automatic Gain Control).

6.10 MERITS AND DEMERITS OF FET

Merits of FET

1. It is less noisy
2. It has high input impedance
3. It is thermally stable
4. It is simple to construct
5. It is immune to radiation
6. It is an useful voltage controlled device
7. It can be used as a voltage variable resistor
8. It is compatible for the fabrication in integrated circuits and occupies less space.

Demerits of FET

1. Its gain bandwidth product is small.
2. Its voltage gain is small.

6.11 ADVANTAGES OF JFET

1. A very high input impedance order of 100Ω .
2. Operation of JFET depends on the bulk material current carriers that do not cross junctions.
3. Very high power gain.
4. Negative temperature coefficients.
5. Smaller size longer life and high efficiency.

6. AC drain resistance r_d it is the ratio of change in drain-source voltage to the change in drain current at constant gate source voltage.
7. The amplification factor is the ratio of change in drain source voltage to the change in gate source voltage at constant drain current.
8. Transconductance is the ratio of change in drain current to the change in gate source voltage at constant drain source voltage.

6.12 APPLICATIONS OF JFET

1. JFETs are used in current sources.
2. JFETs are used as voltage controlled resistance devices.
3. JFETs are used in buffer voltage amplifiers.
4. JFETs are used in analog and digital switches.
5. JFETs are used in very high resistance amplifiers.

6.13 FET COMMON SOURCE AMPLIFIER

Common source amplifier is one with no source resistor, so the source is connected to the ground. Common source amplifier is widely used and is similar to CE of a BJT. Circuit configuration as shown in figure 6.15. Common source FET configuration is probably the most widely used of all FET circuit configurations.

Common Source (CS) amplifier is the FET equivalent of the common emitter transistor amplifier configuration. Like the CE amplifier, it is capable of high voltage gain. The CS amplifier has the input applied between the gate and source terminals and the output signal taken across the drain and source terminals. Therefore, the source terminal is common to both the input and output signals. Small signal equivalent circuit using the voltage source model of FET as shown in figure 6.15.

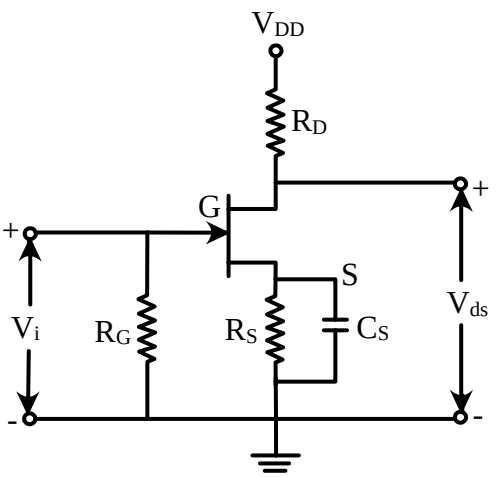


Figure 6.15: Common Source Amplifier

Voltage Gain: The source resistor (R_S) can be used to set the Q point bus is by passed by CS for mid frequency operation. The output voltage for small signal equivalent circuit is,

$$V_0 = \frac{-R_D}{R_D + r_d} \mu V_{gs}$$

Where $V_{gs} = V_i$, the input voltage.

The voltage gain, $A_V = \frac{V_o}{V_i} = -\frac{\mu R_D}{R_D + r_d}$

Here, negative sign indicates the phase shift of 180° between input voltage and output voltage.

Input Impedance: The input impedance for CS amplifier is, $Z_i = R_G$

For the voltage divider bias as in CE amplifiers of BJT is, $R_G = R_1 \| R_2$

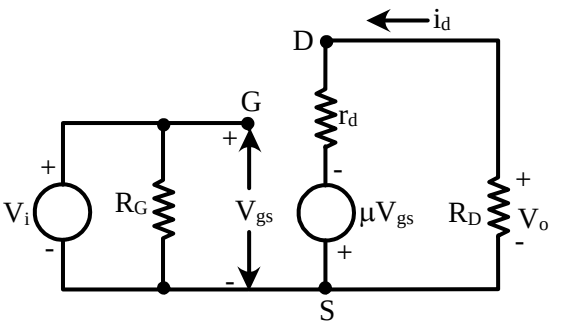


Figure 6.16: Small signal equivalent circuit of CS amplifier

Output Impedance: It is the impedance at the output terminals with the input voltage $V_i = 0$. When $V_i = 0$, $V_{gs} = 0$ and hence $\mu V_{gs} = 0$

The equivalent circuit is as follows for calculating output impedance.

Output impedance is $Z_0 = r_d \| R_D$

Hence, normally r_d will be far greater than R_D.

Hence $Z_0 \approx R_D$.

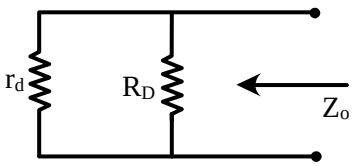


Figure 6.17: Calculation of output impedance

Note

1. Voltage gain, $A_V = \frac{V_o}{V_i} = -\frac{\mu R_D}{R_D + r_d}$
2. The input impedance is given by, $Z_i = R_G$
3. The output impedance is given by, $Z_0 = r_d \| R_D \approx R_D$.

6.14 FET COMMON DRAIN AMPLIFIER

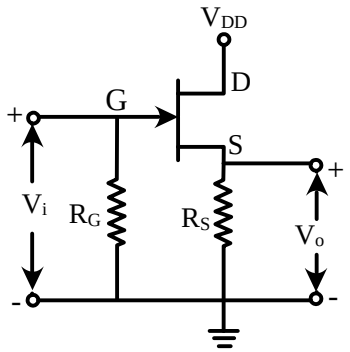


Figure 6.18: Common Drain amplifier

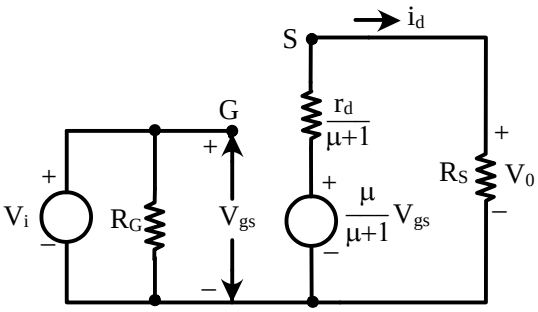


Figure 6.19: Small signal equivalent circuit of CD amplifier

Common Drain Amplifier: Common drain amplifier is similar in configuration to common collector of BJT. This is also referred to source follower. The circuit of such an amplifier is as shown in figure 6.18 and figure 6.19 shows that the small signal equivalent circuit of CD amplifier.

Like the transistor emitter follower, the source follower configuration itself provides a high level of buffering and the high input impedance. Actual input resistance of a FET itself is very high as it is a field effect device. It means the source follower circuit is able to provide an excellent performance as a buffer. Voltage gain is unity, although current gain is high. The input and output signals are in phase. Various parameters of the amplifier can be determined by the following.

Voltage Gain

The voltage gain is, $A_V = \frac{V_o}{V_i}$ ... (1)

Here, $V_o = \frac{R_S}{R_S + \frac{r_d}{\mu+1}} \times \frac{\mu}{\mu+1} V_{gd} = \frac{\mu R_s V_{gd}}{(\mu+1)R_s + r_d}$

Since, $V_i = V_{gd}$

Substituting the above values in equation (1). We get,

$$\therefore A_V = \frac{V_0}{V_i} = \frac{\frac{\mu R_S V_{gd}}{(\mu+1)R_S + r_d}}{V_{gd}} = \frac{\mu R_S}{(\mu+1)R_S + r_d}$$

In CD configuration there is no phase shift between output voltage and input voltage.

Input Impedance: $Z_i = R_G$

Output Resistance: It is measured at the output terminals with an input voltage $V_i = 0$ can be simply calculated from the following equivalent circuit.

As $V_i = 0$, $V_{gd} = 0$, $\frac{\mu}{\mu+1} V_{gd} = 0$

$$Z_0 = \frac{r_d}{\mu+1} \| R_S$$

If $\mu >> 1$

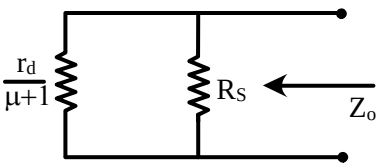


Figure 6.20: Calculation of output impedance

The voltage gain is slightly less than unity. It implies that an output voltage at the source follows the input voltage at the gate. CD amplifier is is thus referred to as source follower and it finds same application as an emitter follower configuration of the bipolar junction transistor.

$$\therefore Z_0 = \frac{r_d}{\mu} \| R_S = \frac{1}{g_m} \| R_S \cdot$$

Note

1. Voltage gain,
$$A_V = \frac{\mu R_S}{(\mu+1)R_S + r_d}$$
2. The input impedance is given by, $Z_i = R_G$
3. The output impedance is given by,
$$Z_0 = \frac{r_d}{\mu} \| R_S = \frac{1}{g_m} \| R_S \cdot$$

6.15 FET COMMON GATE AMPLIFIER

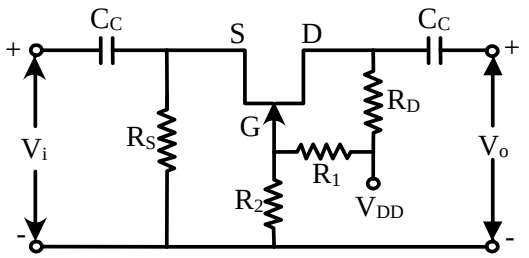


Figure 6.21: Common gate amplifier

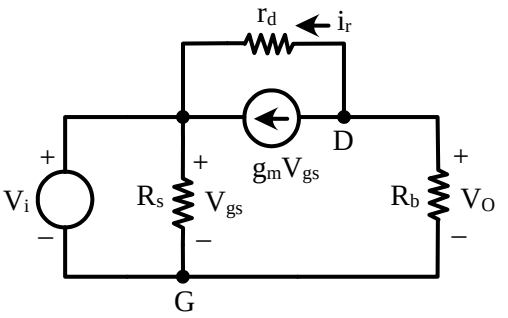


Figure 6.22: Small signal equivalent circuit of CG amplifier

Common Gate Amplifier: FET in common gate configuration can be used as high frequency amplifier. The circuit of such a configuration is as shown in figure 6.21 and figure 6.22 as shows that the small signal equivalent circuit of a CG amplifier. In a CG amplifier, the input signal is applied to the source and the output signal is taken from a drain.

We can replace the FET with its small signal model to determine the various parameters of a CG amplifier. Modified equivalent circuit is as shown in figure 6.23.

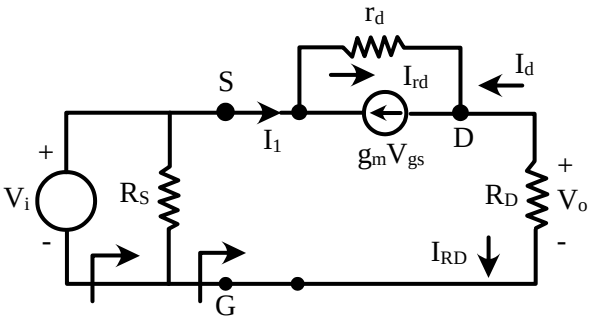


Figure 6.23: Modified equivalent circuit

Voltage Gain: From figure 6.22, by applying KCL,

$$i_r = i_d - g_m V_{gs}$$

By applying KVL,

$$V_o = \left(i_d - g_m V_{gs}\right) r_d + V_{sg}$$

$$V_{sg} = -V_{gs} = V_i \text{ and } i_d = \frac{-V_o}{R_D}$$

$$V_o = \left(\frac{-V_o}{R_D} + g_m V_i\right) r_d + V_i$$

$$A_V = \frac{V_o}{V_i} = \frac{\left(g_m r_d + 1\right) R_D}{R_D + r_d}$$

Input Impedance: From figure 6.22 and 6.23

The current through r_d is, $I_{rd} = -I_r = I_1 + g_m V_{gs}$ … (1)

But $I_1 = I_{rd} - g_m V_{gs}$ … (2)

$$I_{rd} = \frac{V_i - V_o}{r_d} = \frac{V_i - I_{RD} R_D}{r_d}$$

Substituting above values in equation (2). We get,

$$I_1 = \frac{V_i - I_{RD}R_D}{r_d} - g_m V_{gs}$$

From figure 6.23, Input Voltage is, $V_i = -V_{gs}$

$$I_1 = \frac{V_i - I_{RD}R_D}{r_d} + g_m V_i = \frac{V_i}{r_d} - \frac{I_{RD}R_D}{r_d} + g_m V_i$$

$$I_1 + \frac{I_{RD}R_D}{r_d} = \frac{V_i}{r_d} + g_m V_i \quad \ldots (3)$$

$$\frac{I_1 r_d + I_{RD}R_D}{r_d} = \frac{V_i}{r_d} + g_m V_i \quad \ldots (4)$$

From figure 6.23, $I_1 = I_{RD}$ in equation (3),

$$\frac{I_1 r_d + I_1 R_D}{r_d} = \frac{V_i}{r_d} + g_m V_i$$

$$I_1\left[\frac{r_d + R_D}{r_d}\right] = V_i\left[\frac{1}{r_d} + g_m\right] \Rightarrow I_1\left[\frac{r_d + R_D}{r_d}\right] = V_i\left[\frac{1 + r_d g_m}{r_d}\right]$$

$$\frac{V_i}{I_1} = \frac{r_d + R_D}{1 + g_m r_d} = Z_i'$$

Here $Z_i = R_S \parallel Z_i'$

$$Z_i = R_S \parallel \frac{r_d + R_D}{1 + g_m r_d}$$

$g_m r_d >> 1$ and $r_d >> R_D$. Then,

$$Z_i = R_S \parallel \frac{r_d}{g_m r_d} = R_S \parallel \frac{1}{g_m}$$

The input impedance is, $Z_i = R_S \,//\, \frac{1}{g_m}$

Output Impedance

The output impedance is, $Z_o = r_d \parallel R_D$

$$Z_o \approx R_D \text{ [Since } r_d >> R_D \text{].}$$

Note

1. Voltage gain,
$$A_V = \frac{(g_m r_d + 1)R_D}{R_D + r_d}$$
2. The input impedance is given by, $Z_i = R_S \,//\, \frac{1}{g_m}$
3. The output impedance is given by, $Z_o \approx R_D$.

6.16 COMMON SOURCE JFET AMPLIFIERS

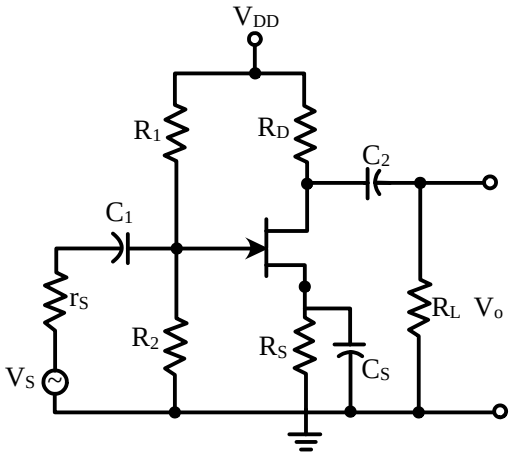


Figure 6.24: Common Source JFET amplifiers

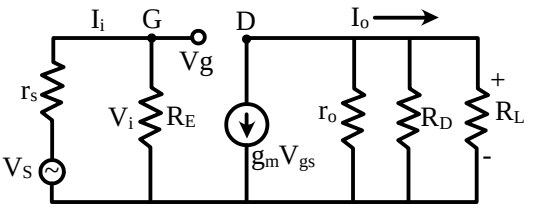


Figure 6.25: Equivalent circuit for CS JFET amplifier

Figure 6.24 shows a JFET CS amplifier arrangement. Here, an resistors R_1, R_2 and R_S provides the stable operating point over a wide range of a temperature and the transfer characteristics.

Capacitors C_1, C_2 and C_S can be assumed to have the reactance's in a operating frequency range that are small compared with $R_1 \parallel R_2, R_L$ and R_S.

The equivalent circuit for JFET CS amplifier as shown in figure 6.25.

From the equivalent circuit for JFET CS amplifier,

The output voltage is,

$$V_o = -g_m V_{gs}(r_o \parallel R_D \parallel R_L) = -g_m V_i(r_o \parallel R_D \parallel R_L) \quad \ldots (1)$$

Voltage Gain: The voltage gain is,

$$A_V = \frac{V_o}{V_i} = -g_m(r_o \parallel R_D \parallel R_L) \quad \ldots (2)$$

The voltage gain, source resistance into consideration as,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_B}{r_s + R_B} x A_V = \left(\frac{R_B}{R_B + r_s}\right) g_m(r_o \parallel R_D \parallel R_L) \quad \ldots (3)$$

In FET amplifiers R_B is very large and r_o is also high.

$$A_V = A_{VS} = -g_m(R_D \parallel R_L) \quad \ldots (4)$$

Input Impedance (Z_i)

The input impedance is,

$$Z_i = \frac{V_i}{I_i} = R_B = R_1 \parallel R_2 \quad \ldots (5)$$

Current Gain A_i

$$A_i = \frac{I_O}{I_i} = \frac{V_o / R_L}{V_i / Z_L} = A_v . \frac{Z_i}{R_L} \quad \ldots (6)$$

Output Impedance Z_o

$$Z_o = r_o \| R_D \| R_L \quad \ldots (7)$$

6.17 COMPARISON OF CS, CD AND CG FET AMPLIFIERS

CS Amplifiers	CD Amplifiers	CG Amplifiers
Voltage gain is, $A_V = \frac{V_o}{V_i} = -\frac{\mu R_D}{R_D + r_d}$	Voltage gain is, $A_V = \frac{\mu R_S}{(\mu+1)R_S + r_d}$	Voltage gain is, $A_V = \frac{(g_m r_d + 1)R_D}{R_D + r_d}$
Input impedance is, $Z_i = R_G$	Input impedance is, $Z_i = R_G$	Input impedance is, $Z_i = R_S // \frac{1}{g_m}$
Output impedance is, $Z_0 = r_d \| R_D \approx R_D$.	Output impedance is, $Z_0 = \frac{r_d}{\mu} \| R_S = \frac{1}{g_m} \| R_S$.	Output impedance is, $Z_o \approx R_D$.
Phaseshift of CS amplifier is 180^0.	Phaseshift of CD amplifier is 0^0.	Phaseshift of CD amplifier is 0^0.
Gain of CS amplifier is generally greater than one.	Gain of CD amplifier is slightly less than one.	Gain of CG amplifier offers gain of more than one.
Output resistance of CS can be determined by R_D .	Output resistance of CD is low $\approx 100\Omega$.	Output resistance of CC can be determined by R_D .
It can be used as a invert input.	It can be used as a voltage buffer.	It can be used as a current buffer.

6.18 SOLVED PROBLEMS

Example-1: A common source FET amplifier circuit shown in figure 6.26 with unbypassed R_S has the following circuit parameters $R_d = 15\,k\Omega$, $R_S = 0.5\,k\Omega$, $R_g = 1M\Omega$, $g_m = 5m$ mho and $V_{DD} = 20\,V$. Calculated amplification parameter A_V and R_o.

Sol.

Given data,

For a common source FET amplifier,

$R_d = 15\,k\Omega$, $R_S = 0.5k\Omega$, $R_g = 1M\Omega$ and $r_d = 5k\Omega$

$g_m = 5m$ mho, $A_V = ?$, $R_o = ?$

We know,

1. Amplification Factor

$$\mu = r_d g_m = 5\times10^3 \times 5\times10^{-3} = 25$$

2. Voltage Gain

$$A_V = \frac{V_o}{V_i} = -\frac{\mu R_D}{R_D + r_d} = -\frac{25\times15\times10^3}{15\times10^3 + 5\times10^3}$$

$$A_V = -\frac{375\,x\,10^3}{20\,x\,10^3} = -18.75$$

3. Output Resistance

Output resistance is, $R_o = R_d \| r_d$

$$R_o = \frac{R_d \times r_d}{R_d + r_d} = \frac{15\times10^3 \times 5\times10^3}{15\times10^3 + 5\times10^3} = \frac{75\,x\,10^6}{20\,x\,10^3}$$

$$\therefore R_o = 3.75\ k\Omega$$

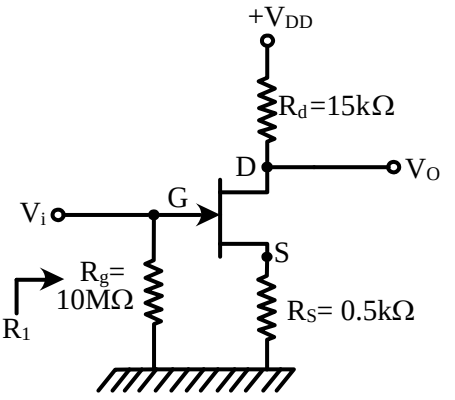


Figure 6.26

Example-2: In the CD amplifier circuit, let $R_S = 4k\Omega$, $R_G = 10M\Omega$, $\mu = 50$ and $r_d = 35k\Omega$. Evaluate the voltage gain A_V, input impedance Z_i and output impedance Z_0.

Sol.

Given data,

$R_S = 4k\Omega$, $R_G = 10M\Omega$, $\mu = 50$ and $r_d = 35k\Omega$

1. Voltage Gain

The voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_S}{(\mu+1)R_S + r_d} \qquad \text{... (1)}$$

Substituting the given values in equation (1). We get,

$$A_V = \frac{50\,x\,4\,x10^3}{(50+1)\,x\,4\,x10^3 + 35\,x10^3} = 0.0836$$

The positive value indicates that V_0 and V_i are in phase and further note that $A_V < 1$ for CD amplifier.

2. Input Impedance

The input impedance is, $Z_i = R_G = 10M\Omega$

3. Output Impedance

Output impedance, $Z_0 = \left(\frac{1}{g_m}\right) \| R_S = \left(\frac{r_d}{\mu}\right) \| R_S$

$$Z_0 = \frac{35\,x\,10^3}{50} \| 4\,x\,10^3 = 595.7\Omega\ .$$

Example-3: In the CG amplifier, let $R_D = 3k\Omega$, $R_S = 2\,k\Omega$, $g_m = 1.43x10^{-3}$mho and $r_d = 20k\Omega$. Evaluate Voltage gain, A_v, input impedance Z_i and output impedance Z_o.

Sol.

Given data,

$R_D = 3k\Omega$, $R_S = 2\,k\Omega$, $g_m = 1.43x10^{-3}$mho and $r_d = 20k\Omega$

1. Voltage Gain A_v

The voltage gain is, $A_V = \dfrac{(g_m r_d + 1)R_D}{R_D + r_d}$

$$A_v = \frac{(1.43x10^{-3}x20x10^3 + 1)3x10^3}{(3x10^3 + 20x10^3)} = \frac{(1.43x20+1)3x10^3}{23x10^3} = 3.86$$

2. Input Impedance: The input impedance is,

$$Z_i = R_S // \frac{1}{g_m}$$

$$2x10^3 \parallel \frac{1}{1.43x10^{-3}} = 2x10^3 \parallel \frac{10^3}{1.43}$$

$$= \frac{2x10^3 x \frac{10^3}{1.43}}{2x10^3 + \frac{10^3}{1.43}} = \frac{2x10^3 x10^3}{2x10^3 x1.43 + 10^3} = 0.5\,k\Omega$$

3. Output Impedance

The output impedance is, $Z_o \approx R_D \approx 3k\Omega$

Example-4: A JFET has $I_{DSS} = 6mA$ and $V_{GS(off)} = -2.5V$. Calculate drain current at $V_{GS} = -1V$.

Sol.

Given data,

$I_{DSS} = 6mA$, $V_{GS(off)} = -2.5V$ and $V_{GS} = -1V$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{... (1)}$$

Substituting the given values in equation (1). We get,

$$\therefore\ I_D = 6\times10^{-3}\left[1 - \frac{1}{2.5}\right]^2 = 6\times10^{-3}\times0.36 = 2.16\,mA$$

Example-5: The drain current of JEET shown in figure 6.27 is given by $I_D = 10\left(1 + \dfrac{V_{GS}}{4}\right)^2$ mA.

Calculate the quiescent values of I_{DS}, V_{DS} and V_{GS}.

Sol.

Given equation is,

$$I_D = 10\left(1+\frac{V_{GS}}{4}\right)^2 \text{ mA} \quad \text{... (1)}$$

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \quad \text{... (2)}$$

Comparing the equation (1) with the standard form equation (2), we get

$I_{DSS} = 10\,\text{mA}; \qquad V_P = -4\text{V}$

Where V_{GS} = Voltage drop cross

$R_S = -I_D \times 500$

Substituting the V_{GS} in the given equation (1). We get,

$$I_D = 10\left[1-\frac{500I_D}{4}\right]^2$$

$$I_D = 10 - 2.5I_D + 0.156I_D^2 \quad \text{... (3)}$$

By solving equation (3). We get,

$I_D = 19.00\,\text{mA}$ (or) 3.36 mA

The first value is absurd as it leads to

$V_D = I_D(R_D - IR_S) = 104\text{V}$

$\therefore I_D = 3.36\text{mA}$

$\therefore\ V_{GS} = -I_D \times 0.5\text{k} = 1.68\text{V}$

$\therefore\ V_{GS} = 30 - 3.36\times10^{-3}(5\text{k}+0.5\text{k}) = 11.52\text{V}$

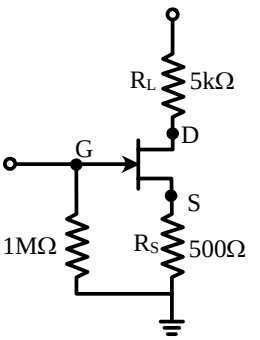


Figure 6.27

Example-6: For a P-channel JFET the physical width of the channel is $2\text{x}10^{-1}$cm and channel resistivity is $20\Omega\text{cm}$. Determine the pinchoff voltage.

Sol.

Given data, $2a = 2\text{x}10^{-1}\text{cm} \Rightarrow a = 1\text{x}10^{-1}\text{cm}$

Now $\sigma = N_D q\mu_n$

$$\rho = \frac{1}{N_D q\mu_n}$$

$$N_D = \frac{1}{20\text{x}1.6\text{x}10^{-19}\text{x}3800} = 8.23\text{x}10^{-13}$$

$$V_P = \frac{qN_D}{2\varepsilon}a^2$$

$$\therefore\ V_P = \frac{1.6\text{x}10^{-19}\text{x}8.23\text{x}10^{13}}{2\text{x}12\text{x}8.85\text{x}10^{-12}}\text{x}10^{-8} = 6.12\text{V}$$

Example-7: Calculate the dynamic resistance of a JFET having amplification factor 80 and transconductance $200\mu mho$.

Sol.

Amplification factor $\mu = 80$

Transconductance $g_m = 200x10^{-6}\,mho$

Dynamic resistance $r_d = ?$

$\mu = g_m x r_d$.

$$\therefore\ r_d = \frac{\mu}{g_m} = \frac{80}{200x10^{-6}} = 400x10^3\Omega = 400k\Omega$$

Example-8: Determine the pinch-off voltage for n-channel silicon FET with a channel width of $5.6x10^{-4}cm$ and a donor concentration of $10^{15}cm^{-3}$. Given that dielectric constant for Si is 12.

Sol.

We know,

$$V_P = \frac{eN_D}{2\varepsilon}a^2$$

Here $2a = 5.6x10^{-4}cm = 5.6x10^{-6}cm$

$\varepsilon = 12\varepsilon_0 = 12x8.86x10^{-12}\,F/m$

$N_D = 10^{15}cm^{-3} = 10^{21}m^{-3}$

Since $e = 1.6x10^{-19}$ coulomb

$$V_P = \frac{1.6x10^{-19}x10^{21}}{2x12x8.86x10^{-12}}x\left(2.8x10^{-6}\right)^2 = 5.9V$$

Example-9: N-Channel JFET has a pinch-of voltage off -4.5V and $I_{DSS} = 9mA$. At what value of V_{GS} in the pinch-off region will I_D be equal to 3mA?

Sol.

The Shockley equation is,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$3 = 9\left(1-\frac{V_{GS}}{-4.5}\right)^2 \Rightarrow \frac{3}{9} = \left(1+\frac{V_{GS}}{4.5}\right)^2$$

$$1+\frac{V_{GS}}{4.5} = \frac{1.732}{93} = 5.777$$

$$\frac{V_{GS}}{4.5} = 0.577 - 1 = -0.423$$

$$V_{GS} = -0.423x4.5 = -1.9V$$

Example-10: In a field effect transistor when value of gate voltage is changed from (-3.0) V to (-2.9)V, the drain current increases for 1mA to 1.2mA. Determine the mutual conductance of the transistor.

Sol.

The mutual conductance

$$\therefore g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{(1.2-1)\text{mA}}{-2.9-(-3)\text{V}} = 2\text{mS}.$$

Check your Knowledge

1. Describe the construction and working of N-channel FET.

Ans. _____

_____

_____

2. Define drain resistance (r_d), transconductance (g_m), amplification factor (μ) and obtain relation among them.

Ans. _____

_____

_____

3. Comparison of characteristics of FET amplifiers.

Ans. _____

_____

_____

4. Discuss small signal model of FET and its parameters.

Ans. _____

_____

_____

5. Explain the output and transfer characteristics of JFET. Explain how a JFET is superior to BJT?

Ans. _____

_____

_____

6. Define FET parameters and give the relationship among them.

Ans. _____

_____

_____

7. Draw the schematic representation of N-channel and P-channel FETs.

Ans. _____

_____

_____

8. Explain the construction of JFET. Describe its drain characteristics showing Ohmic region and pinch-off region.

Ans. _____

_____

_____

9. Give the working mechanism of a FET.

Ans. _____

_____

_____

10. Describe the operation of FET and draw its output characteristics.

Ans. _____

_____

_____

6.19 FET Biasing

The biasing of a field effect transistor is not as critical as of biasing a bipolar junction transistor since the operating point selection in a FET is base only on three parameters, namely, I_D, V_{GS}, V_{DS} whereas for a BJT the dimensions of operating point should be selected in the constant current region.

It is necessary to maintain the operating point Q stable in the central portion of the pinch voltage region in FET biasing. The Q-point should be independent of device parameter variations and an ambient temperature changes. It can be achieved by suitable selecting the gate to source voltage and drain current which is referred to as biasing.

Biasing an FET amplifier circuit is similar to BJT amplifiers. We will use components external to transistor and dc sources to define a predictable and stable operating point, about which the circuit may provide linear amplification. Bias stability in FET amplifiers means that the dc drain current (ID) stays as constant as possible with variations in operating conditions and device parameters. The different biasing techniques are,

1. Fixed bias method
2. Self -bias method
3. Voltage divider bias method

The purpose of all the four biasing techniques is to provide a stable Q point in the constant current or saturation region of JFET's output characteristic against widespread variations in parameters of a JFET due to the fabrication variations and temperature fluctuations.

The variation of 50% in the parameters of JFET is not unusual. To ensure that Q-point is in the constant current or saturation region. The care must be taken to see that quiescent value of $|V_{DS}|$. The drain-to-source voltage must be greater than $|V_P| - |V_{GS}|$, where V_{GS} is gate-to-source voltage and region by the JFET's equation of the form is,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The I_{DSS} is drain current with the gate source terminal shorted.

6.19.1 Fixed-Bias Configuration

The FET device needs the DC bias to setting of gate-source voltage V_{GS} to give the desired drain current I_D. For the JFET drain current is limited by the saturation current I_{DSS}. Thus, the FET has such a high input impedance and it does not allow the gate current to flow and the dc voltage of the gate set by a voltage divider or the fixed battery voltage is not affected or loaded by FET.

The fixed dc bias can be obtained by using the battery V_{GG}. This battery can be ensures that the gate is always negative with respect to source and no current flows through resistor R_G and gate terminal i.e., $I_G = 0$.

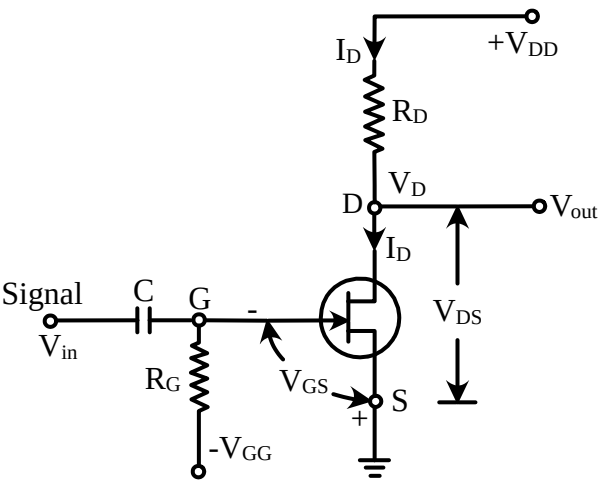


Figure 6.28: Fixed biasing circuit for JFET

The battery provides a voltage V_{GS} to bias the N-channel JFET but no resulting current can be drawn from the battery V_{GG}. The Resistor R_G is included to allow any ac signal applied through capacitor C to develop across R_G. Any ac signal will develop across R_G and the dc voltage drop across R_G is equal to $I_G R_G$ i.e., 0 volt.

The gate-source voltage V_{GS} is,

$$V_{GS} = -V_G - V_S = -V_{GG} - 0 = -V_{GG} \quad \text{... (1)}$$

The drain-source current I_D is then fixed by the gate-source voltage as determined by equation. This current causes a voltage drop across the drain resistor R_D and is,

$$V_{DD} = I_D R_D + V_{DS} \quad \text{... (2)}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

We know that JFET always operates in depletion mode i e., '$V_{GG} = -Ve$'

By applying KVL at input circuit, we get $V_{GG} = -V_{GS}$

By applying KVL at output circuit, we get $V_{DS} = V_{DD} - I_D R_D$

6.19.2 Self-Bias Configuration

The basic circuit of the N-channel FET self biased configuration has been shown in figure 6.29. This is the most common method for biasing a JFET. Hence, no gate current flows through the reverse-biased gate-source, the gate current $I_G = 0$. Therefore,

$$V_G = I_G R_G = 0V$$

With a drain current I_D and at the voltage source S is,

$$V_S = I_D R_S \quad \text{... (1)}$$

The drain volatge is $V_D = V_{DD} - I_D R_D$

The gate-source voltage is, $V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$ ... (2)

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S) \quad \text{... (3)}$$

$$I_D [R_D + R_S] = V_{DD} - V_{DS}$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D + R_S}$$

If $I_D = 0 \quad V_{DD} = V_{DS}$

If $V_{DS} = 0 \Rightarrow I_D = \frac{V_{DD}}{R_D + R_S}$ ... (4)

The voltage V_{GS} and no external source is required for biasing and this is the reason it is called as self-biasing. DC conditions of JFET amplifier is fully specified. Self biasing of a JFET stabilizes its quiescent operating point against any change in its parameters like transconductance.

Consider the given JFET can be replaced by another JFET having the double conductance then drain current will also try to be double but since any increase in voltage drop across R_S. Hence, the gate-source voltage V_{GS} becomes more negative and thus increase in drain current can be reduced.

From equation (4), I_D increase then the voltage drop across the resistor increases.

- If I_D is current is high then the drop across, the resistor R_S is also very high.

  $I_S R_S = V_S = I_D R_S \uparrow$

  Therefore V_{GG} also increases negatively $(V_{GG} = -V_S)$

The channel width decreases, finally the drain current decreases. Suppose if the drain current is very low then the drop across the resistance R_S is also very low. Therefore V_{GG} is also very low.

6.19.3 Voltage Divider Bias

Figure 6.29 (a) shows the voltage divider bias circuit and its Thevenin's equivalent circuit as shown in figure 6.29(b). Resistors R_1 and R_2 can be connected on gate side forms the voltage divider.

The gate voltage is,

$$V_{GG} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} \text{ and } R_g = \frac{R_1 R_2}{R_1 + R_2}$$

The circuit can be reduced.

The bias line satisfies the equation is,

$$V_{GS} = V_{GG} - I_D R_S$$

Drain to ground voltage is, $V_D = V_{DD} - I_D R_D$

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$
$$= I_D R_D + V_{DS} + I_D R_S$$
$$V_{DD} = I_D (R_D + R_S) + V_{DS}$$

If the gate voltage V_{GG} is very large as compared to gate to source voltage V_{GS} and the drain current is approximately constant. The voltage divider bias is less effective with the JFET than BJT.

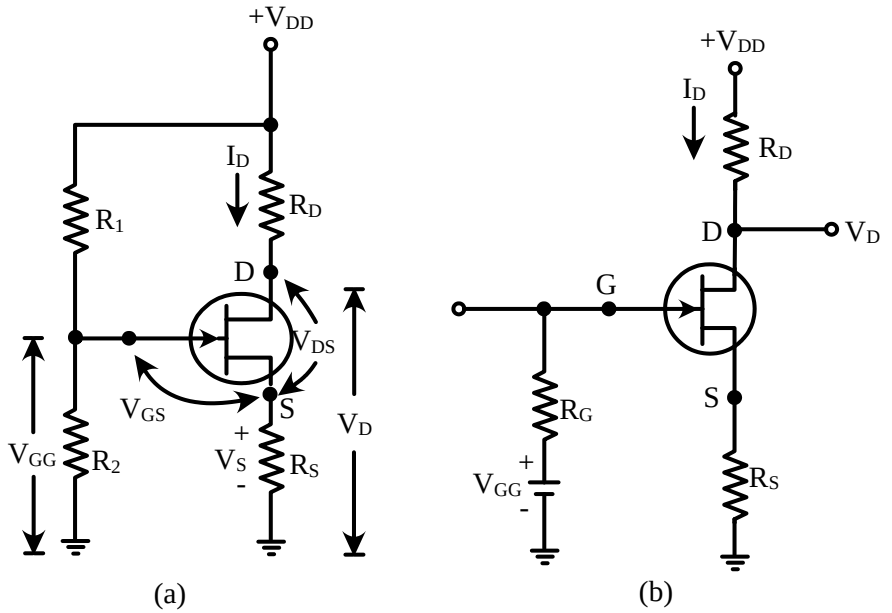


Figure 6.29: (a) Voltage divider bias circuit and (b) Thevenin's equivalent circuit

This is because in BJT, $V_{BE} \approx 0.7V$ (Si) with only minor variations from one transistor to another. But in JFET, V_{GS} can vary several volts from one JFET to another.

6.19.4 Potential Divider Biasing

The slightly modified form of dc bias is provided by the circuit as shown in figure 6.30. The resistors R_{G1} and R_{G2} form the potential divider across drain supply V_{DD}. The voltage V_2 across R_{G2} provides the necessary bias as shown in figure 6.30. The additional gate resistor R_{G1} from gate to supply voltage can be facilitates in larger adjustment of dc bias point and permits use of larger valued R_S.

The gate is reverse biased so that $I_G = 0$ and gate voltage is,

$$V_G = V_2 = (V_{DD} / R_{G1+}R_{G2}) x R_{G2}$$

$$V_{GS} = V_G - V_S = V_G - I_D R_S \quad \text{... (1)}$$

The circuit is so designed that $I_D R_S$ is greater than V_G so that V_{GS} is negative. It can be provides correct bias voltage. The operating point can be determined as,

$$I_D = (V_2 - V_{GS}) / R_S$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \quad \text{... (2)}$$

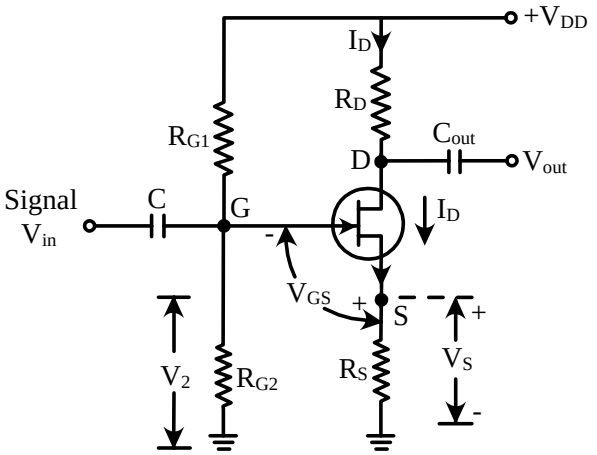


Figure 6.30: Potential Divider Bias Circuit for N-Channel JFET

Check your Knowledge

1. Explain in detail about different biasing techniques.

Ans. _____

_____

_____

2. Write in detail about voltage divider bias and potential divider bias.

Ans. _____

_____

_____

6.20 OUTCOMES

- Able to design a JFET based amplifier for practical applications.
- Ability to perform analysis on various configuration of JFET.
- Select a suitable biasing method for the JFET stability.

6.21 SUMMARY

The FETs are unipolar devices because they operate only with one type of charge carrier. P-channel JFET's channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types. Since electrons have a higher mobility through a conductor compared to holes. The input impedance of FET is more than that of BJT because the input circuit of FET is reverse bias whereas the input circuit of BJT is forward bias.

FET amplifiers have certain advantages over BJT amplifiers like high input impedance. However, the BJT normally has a higher voltage gain. These are also similarities in the three amplifier configurations of FETs and BJTs. Common-drain has no phase shift, the gain slightly less than 1 and the output is taken from the source. Common-gate has no phase shift and low input resistance. FET amplifier configuration is similar to BJT amplifiers. Trans-conductance (g_m) relates the drain current (ac output) to the ac input voltage (V_{gs}). The input resistance for a FET at the gate is extremely high. Common-source is the most used type of a FET amplifier and has a phase inversion is 180^o.

6.22 REVIEW QUESTIONS

I. Short Answer Questions

1. Distinguish between BJT and FET.
2. Discuss the advantages of FET over BJT.
3. Write the advantages and disadvantages of JFET over BJT.
4. In what respect does a FET differ from a BJT?
5. Give the working mechanism of a FET.
6. Explain the differences between biasing a BJT and a FET.
7. Explain the methods used for biasing JFET.

8. Define pinch-off voltage of a JFET. Sketch the depletion region before and after pinch off.
9. Describe the operation of FET and draw its output characteristics.
10. Sketch small signal FET model.
11. Describe the construction and working of N-channel FET.
12. Describe construction and working of JFET.
13. Define drain resistance (r_d), transconductance (g_m), amplification factor (μ) and obtain relation among them.
14. Define the amplification factor.
15. Comparison of performance quantities of the FET amplifiers.
16. Comparison of characteristics of FET amplifiers.

II. Long Answer Qusetsions

1. Explain the construction, working and V-I characteristics of JFET.
2. Draw the schematic representation of N-channel and P-channel FETs.
3. Explain with a neat circuit diagram, an experiment to determine the output and transfer characteristics of a FET.
4. Explain the construction and working of a FET. How do you determine its characteristics?
5. Explain the construction and characteristics of a JFET. Give its small signal model and explain the different terms used.
6. Mention three important differences between a transistor and a FET as circuit element. Give the experimental set up for FET characteristics and discuss them.
7. Discuss the output and transfer characteristics of FET with experimental set-up.
8. Discuss small signal model of a FET. Draw its small signal equivalent circuit.
9. Discuss small signal model of FET and its parameters.
10. Explain the terms, pinch-off voltage, ON-resistance and pinch-off region.
11. Define FET parameters and give the relationship among them.
12. Describe the experimental set up to draw the output and transfer characteristics of a JFET. Explain how FET parameters are determined from these characteristics.
13. Describe the experimental setup to draw the output and transfer characteristics of JFET. Explain how FET parameters can be determined from these characteristics?
14. Explain the output and transfer characteristics of JFET. Explain how a JFET is superior to BJT?
15. Describe the construction and working of JFET with a neat diagram. Explain its various biasing modes.

16. Explain experimental arrangement for studying output and transfer characteristics and to determine FET parameters.
17. Explain the construction of JFET. Describe its drain characteristics showing Ohmic region and pinch-off region.
18. Derive the expressions for FET as a common source amplifiers.
19. Derive the expressions for FET as a common drain amplifiers.
20. Derive the expressions for FET as a common gate amplifiers.
21. Explain in detail about generalized FET Amplifiers.
22. Derive the expressions for JFET as a common source amplifiers.

III. Exercises

1. Determine the value of R_D and R_S for a self biased P-channel JFET using the following parameters $V_P = 5V$, $I_{DSS} = 12mA$, $V_{DD} = 12V$, $I_D = 5mA$ and $V_{DS} = 6V$.

   [Ans : $R_D = 1.5\Omega, R_S = 525k\Omega$]
2. Determine the values of R_S required in self biased circuit of N-channel JFET with $I_{DSS} = 50mA$, $V_P = -10V, V_{GSQ} = -5V$. **[Ans : 400Ω]**
3. Design a self-bias configuration for a n-channel JFET having $I_{DSS} = 8mA$ and $V_P = -6V$. The Q-point is at $I_{DQ} = 4mA$ with a supply voltage of 14V. Assume $R_D = 3R_S$.

   [Ans : $R_S = 0.43k\Omega, R_D = 1.3k\Omega$]

6.23 MULTIPLE CHOICE QUESTIONS

1. The JFET is a ( )
   (a) Voltage Controlled device (b) Current Controlled device
   (c) Voltage and current Controlled device (d) Regulator device
2. The input resistance of a FET is ___ ( )
   (a) Nearly zero (b) Nearly one (c) Nearly infinite (d) Nearly two
3. The gate-source junction of a JFET should be ( )
   (a) Forward biased (b) Reverse biased
   (c) Either forward or reverse biased (d) In saturation
4. The pinch-off voltage has same magnitude as the ( )
   (a) Gate Voltage (b) Drain source voltage
   (c) Gate source voltage (d) Gate source cut-off voltage

5. For small values of drain to source voltage V_{DS}, a JFET behave like a ( )

   (a) Resistor (b) Constant current

   (c) Constant voltage source (d) None of the above

6. When the gate voltage becomes more negative in n-channel JFET, the channel between the depletion layers ( )

   (a) Shrinks (b) More conducts (c) Expands (d) None

7. An operational amplifier has ( )

   (a) Zero input resistance (b) Infinite input resistance

   (c) Variable input resistance (d) Based on input

8. The voltage follower has a ( )

   (a) Unity gain (b) Infinite gain (c) Zero gain (d) None

9. In a P-channel JFET, the charge carriers are ____ ( )

   (a) Electrons (b) Holes

   (c) Both electrons and holes (d) Either electrons or holes

10. If the reverse bias voltage is increased then the width of the conducting channel of JFET is ( )

    (a) Increased (b) Decreased (c) Remains same (d) None

11. The input control parameter if JFET is ( )

    (a) Source voltage (b) Gate voltage

    (c) Drain voltage (d) Channel

12. The constant current region of a JFET lies between ( )

    (a) Cut-off and saturation (b) Cut-off and pinch-off

    (c) Pinch off and break down regions (d) 0 and I_{DSS}

13. The trans-conductance of a JFET ranges from ( )

    (a) 0.5 to 30mA/V (b) 100 to 500mA/V

    (c) 500 to 750mA/V (d) Above 750mA/V

14. FETs have similar properties to ( )

    (a) PNP transistors (b) NPN transistors

    (c) Themonic valves (d) Unijunction transistors

15. For small values of drain-to-source voltage, JFET behaves like a ( )

    (a) Resistor (b) Constant-current source

(c) Constant-voltage source (d) Negative resistance

16. In a JFET, the primary control on drain current is exerted by ( )

(a) Channel resistance (b) Size of depletion regions

(c) Voltage drop across channel (d) Gate reverse bias

17. In a JFET, as external bias applied to the gate is increased ( )

(a) Channel resistance is increased

(b) Drain current is increased

(c) Pinch-off voltage is reached at lower values of I_D

(d) Size of depletion regions is reduced.

18. The transconductance 'g_m' of a JFET is equal to ( )

(a) $-\frac{2I_{DSC}}{V_P}$ (b) $\frac{2}{|V_P|}\sqrt{I_{DSS}I_D}$

(c) $-\frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$ (d) $\frac{I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$

19. The extremely high input impedance of a MOSFET is primarily due to the ( )

(a) Absence of its channel

(b) Negative gate-source voltage

(c) Depletion of current carriers

(d) Extremely small leakage current of its gate capacitor

20. Threshold voltage of an N-channel enhancement mode MOSFET is 0.5 V, when the device is biased at a gate voltage of 3 V, pinch-off would occur at a drain voltage of ( )

(a) 1.5 V (b) 2.5 V (c) 3.5 V (d) 4.5 V

Answers

1. (a)	2. (c)	3. (b)	4. (d)	5. (a)	6. (a)
7. (c)	8. (a)	9. (b)	10. (b)	11. (b)	12. (c)
13. (a)	14. (b)	15. (a)	16. (d)	17. (c)	18. (c)
19. (d)	20. (c)				