NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

I M.TECH I Semester Regular Examinations, January-2025

R24

Sub Code: R24MCC101 **RESEARCH METHODOLOGY & IPR**
Time: 3 hours (MD,CSE, STRE, PID, DECS, VLSI&ES) Max. Marks: 60

Note: Answer All **FIVE** Questions.
All Questions Carry Equal Marks (5 X 12M = 60M)

Q.No		Questions	KL	CO	M
1		Unit-I			
	a	i) Explain Clearly the objectives of Research Problem	K2	1	6M
		ii) Interpret different sources of research problem by giving suitable examples	K2	1	6M
		OR			
	b	i) Explain clearly research design process and steps to be followed	K2	1	12M
2		Unit-II			
	a	i) How do you design a research problem? Give an example to illustrate your answer	K2	2	6M
		ii) Discuss various issues involved in selecting a research problem. Also elaborate important features of a good research design.	K2	2	6M
		OR			
	b	i) Differentiate between qualitative research and quantitative research	K2	2	12M
3		Unit-III			
	a	i) Explain the procedure to determine the size of sample and discuss on sampling size	K2	3	6M
		ii) Explain the Concepts of Statistical Population	K2	3	6M
		OR			
	b	Explain different types of sampling techniques	K2	3	12M
4		Unit-IV			
	a	i) Explain new developments in Intellectual Property Rights.	K2	4	6M
		ii) Define intellectual property in research. Explain different types of intellectual property	K2	4	6M
		OR			
	b	i) Contrast the purpose and functions of trademarks	K2	4	6M
		ii) Write notes on trade secrets, precautions and maintenance	K2	4	6M
5		Unit-V			
	a	i) Exemplify the basic criteria of patentability of industrial designs	K2	5	6M
		ii) Explain the fundamentals of copyright laws	K2	5	6M
		OR			
	b	i) Describe briefly how the online patent data is organized	K3	5	6M
		ii) Describe the structure and content of a patent document in general.	K3	5	6M

KL: Blooms Taxonomy Knowledge Level CO: Course Outcome M: Marks

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NARASARAOPETA ENGINEERING COLLEGE
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I M. Tech I Semester Regular Examinations, January-2025

Sub Code: R24MNC102 **DISASTER MANAGEMENT**

Time: 3 hours (STRE, P&ID, MD,DECS,VLSI&ES and CSE) Max. Marks: 60

Note: Answer All **FIVE** Questions.

All Questions Carry Equal Marks (5 X 12 = 60M)

Q.No		Questions	KL	CO	M
1		Unit-I			
	a	i) Describe types of disasters with examples.	K2&K3	C01	6M
		ii)) Explain About The Disaster Management Cycle	K2&K3	C01	6M
		OR			
	b	i) Explain how the Richter scale is used to measure the magnitude of an earthquake	K2&K3	C01	6M
		ii) Discuss various types of natural disasters in India and highlight their effects	K2&K3	C01	6M
2		Unit-II			
	a	Explain The causes of Floods and the effects of Floods in detail. Give one Case Study of The Floods.	K2&K3	C02	12M
		OR			
	b	Explain The causes of earthquakes and effects of earthquakes in detail. Give one Case Study of The earthquake.	K2&K3	C02	12M
3		Unit-III			
	a	i) Explain the Earthquake zones of India	K2&K3	C03	6M
		ii) explain assessing risk and vulnerability	K2&K3	C03	6M
		OR			
	b	What is drought? Explain the types of droughts. Explain drought mitigation with an integration of technology and people.	K2&K3	C03	12M
4		Unit-IV			
	a	i) what are the multimedia technologies of disaster risk management in remote sensing	K2&K3	C04	12M
		OR			
	b	i) what are the forewarning levels of disaster management	K2&K3	C04	6M
		ii) Explain About The Mass Media and disaster Management?	K2&K3	C04	6M
5		Unit-V			
	a	i) what are the disaster management acts and policies in India	K2&K3	C05	6M
		ii) What are the steps for formulating a disaster risk reduction plan?	K2&K3	C05	6M
		OR			
		What are favourable conditions for cyclone formation? How do you estimate risk from cyclonic conditions and safety precautions to save lives?	K2&K3	C05	12M

NARASARAOPETA ENGINEERING COLLEGE
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I M.TECH I Semester Regular Examinations, January-2025

R24

Sub Code: R24MVL102 **RTL SIMULATION & SYNTHESIS WITH PLDS**

Time: 3 hours ECE (VLSI-ES) Max. Marks: 60

Note: Answer All **FIVE** Questions.

All Questions Carry Equal Marks (5 X 12M = 60M)

Q.No		Questions	KL	CO	M
1.		Unit-I			
	a	i)Describe various issues in HDL Coding.	2	1	6M
		ii) Differentiate the Top-Down and Bottom-Up design methodologies.	2	1	6M
		OR			
	b	i) State the merits of HDLs over the traditional schematic-based designs.	2	1	6M
		ii) Illustrate the lexical conventions used in Verilog HDL.	2	1	6M
2		Unit-II			
	a	i)Design a logic circuit to perform the addition of two BCD numbers.	3	2	6M
		ii) Derive an algorithm to perform the unsigned binary multiplication.	4	2	6M
		OR			
	b	i) Design a Binary divider.	3	2	6M
		ii) Implement a sequence detector using finite-state machines.	4	2	6M
3.		Unit-III			
	a	i) Explain the key stages of the ASIC design flow. How does the RTL-to-GDSII flow ensure the manufacturability and functionality of an ASIC?	4	3	6M
		ii) Describe the objectives of clock tree synthesis in the ASIC design flow. How do skew and latency impact overall chip performance?	2	3	6M
		OR			
	b	i) What are the challenges associated with the design closure (timing, power, and area) in the ASIC design flow? Illustrate the techniques to mitigate these challenges.	2	3	6M
		ii) Why is functional verification considered a bottleneck in ASIC design? Discuss the role of simulation, formal verification, and emulation in ensuring a bug-free design.	2	3	6M
4.		Unit-IV			
	a	i) What is the difference between Static Timing Analysis and dynamic timing analysis? Why is STA the preferred method for timing verification in modern ASIC design?	2	4	6M
		ii) Explain the key factors influencing gate delay and interconnect delay in STA. How do process variations affect these delays?	2	4	6M
		OR			
	b	i) Define setup and hold timing checks. Why are these constraints critical for ensuring correct functionality in synchronous circuits?	4	4	6M
		ii) Describe the four types of timing paths analyzed in STA. How does the analysis of clock-to-output paths differ from that of input-to-register paths?	2	4	6M
5		Unit-V			
	a	i) Implement the following Boolean functions using PLA. $f_1=\sum m(7,8,9,10,11,12,13,14,15)$ $f_2=\sum m(1,3,8,12,13)$ $f_3=\sum m(0,2,3,4,5,6,7,8,,10,11,15)$	4	5	6M
		ii) Implement a programmable logical device that determines the cube of a given 3-bit number, using PAL	3	5	6M

		OR			
	b	i) Design 16×8 PROM, to implement the Boolean functions $f_1 = \sum m(2,8,10,15)$ $f_2 = \sum m(1,3,8,12)$ $f_3 = \sum m(5,7,9,11,13)$	4	5	6M
		ii) Design a BCD to Excess3 code converter, using PLA.	3	5	6M

KL: Blooms Taxonomy Knowledge Level CO: Course Outcome M:Marks

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NARASARAOPETA ENGINEERING COLLEGE
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I M.TECH I Semester Regular Examinations, January-2025

R24

Sub Code: R24MVL103

MICRO CONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Time: 3 hours | ECE (VLSI-ES) | Max. Marks: 60

Note: Answer All **FIVE** Questions.
All Questions Carry Equal Marks (5 X 12M = 60M)

Q.No			Questions	KL	CO	M
1			Unit-I			
	a	i)	Explain how the ARM Cortex-M3 processor achieves a balance between high performance and low power consumption. Provide examples of applications where this tradeoff is crucial.	2	1	6M
		ii)	Illustrate the ARM Cortex-M3's register set with its purpose and organization. How does this design enhance the processor's performance for embedded programming?	4	1	6M
			OR			
	b	i)	Discuss the advantages of the ARM Cortex-M3's memory protection unit. Provide an example of how the MPU can be used to isolate tasks in an embedded system.	2	1	6M
		ii)	Detail the ARM Cortex-M3's Thumb-2 instruction set. How does it improve code density and execution efficiency compared to the original ARM instruction set?	2	1	6M
2			Unit-II			
	a	i)	Explain the role of the Nested Vectored Interrupt Controller (NVIC) in the ARM Cortex-M3. Provide a programming example demonstrating its usage in handling multiple interrupts.	2	2	6M
		ii)	Describe the exception model of the ARM Cortex-M3 processor. How does it differ from traditional processor architectures?	2	2	6M
			OR			
	b	i)	Discuss the significance of deterministic interrupt latency in real-time applications. How does the ARM Cortex-M3 architecture ensure this, and in which real-world scenarios is this most beneficial?	2	2	6M
		ii)	Analyze the role of the Fault exceptions in ensuring system robustness. Provide scenarios where each fault type might occur.	4	2	6M
3			Unit-III			
	a	i)	Describe the memory hierarchy of the LPC17xx microcontroller. How does the internal memory architecture contribute to its performance in embedded applications?	2	3	6M
		ii)	Write a program to configure Timer 0 in the LPC17xx microcontroller to generate an interrupt every 1 millisecond. Explain the calculation of the pre-scale value.	4	3	6M
			OR			
	b	i)	Discuss the significance of the LPC17xx microcontroller's Memory Mapping Control (MEMMAP) register. How does it influence the behaviour of internal memory regions?	2	3	6M
		ii)	Write a program to simultaneously configure LPC17xx Timer 0 and Timer 1 for independent periodic event generation.	4	3	6M

4	Unit-IV					
	a	i)	Explain the architectural features of a Programmable DSP processor that differentiate it from general-purpose processors. How do these features enhance signal processing efficiency?	2	4	6M
		ii)	Describe the role of pipelining and parallelism in improving the performance of P-DSP processors. How are these concepts implemented in modern DSP architectures?	2	4	6M
	OR					
	b	i)	Discuss the significance of the Multiply-Accumulate (MAC) unit in DSP processors. How does it support real-time digital signal processing applications?	2	4	6M
		ii)	Evaluate the impact of barrel shifters on the execution speed of multiply-accumulate (MAC) operations in P-DSP processors.	4	4	6M
5	Unit-V					
	a	i)	Explain the core principles of VLIW architecture. How does it differ from traditional superscalar and pipelined architectures?	2	5	6M
		ii)	Discuss the concept of instruction-level parallelism (ILP) in VLIW architecture.	2	5	6M
	OR					
	b	i)	Describe the importance of dual data paths in the TMS320C6000 architecture. How do they contribute to the efficient execution of arithmetic and logical operations?	3	5	6M
		ii)	Analyze the purpose and functionality of cross paths in the TMS320C6000 series. How do they facilitate efficient data movement within the processor?	4	5	6M

KL: Blooms Taxonomy Knowledge Level CO: Course Outcome M:Marks

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NARASARAOPETA ENGINEERING COLLEGE
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I M.TECH I Semester Regular Examinations, January-2025

R24

Sub Code: R24MVL106 **VLSI SIGNAL PROCESSING**

Time: 3 hours ECE (VLSI&ES) Max. Marks: 60

Note: Answer All **FIVE** Questions.

All Questions Carry Equal Marks (5 X 12M = 60M)

Q.No		Questions	KL	CO	M
1		Unit-I			
	a	i) Explain the role of the dataflow graph (DFG) in representing the DSP algorithm. Convert $y[n]=0.5\,y[n-1]+x[n]+2x[n-1]$ into a DFG and analyze its critical path.	3	1	6M
		ii) Describe the benefits of DSP algorithms in modern communication systems.	2	1	6M
		OR			
	b	i) Analyze how the programmability and flexibility of DSP algorithms enable their use in adaptive systems.	4	1	6M
		ii) Discuss the role of pipelining in meeting the constraints of real-time DSP systems. Highlight the challenges and solutions associated with latency, synchronization, and resource utilization.	2	1	6M
2		Unit-II			
	a	i) Explain the significance of register minimization techniques in the design of VLSI systems for signal processing.	2	2	6M
		ii) Analyze the effect of the folding factor on register usage in a folded DSP system.	4	2	6M
		OR			
	b	i) Discuss the interplay between retiming and folding transformations for register minimization.	2	2	6M
		ii)How does retiming help reduce register count in folded architectures?	4	2	6M
3		Unit-III			
	a	i) Construct the systolic architecture for the systolic array designed for the convolution operation: $y[n]=\sum_{k=0}^{3} h[k].x[n-k]$	3	3	6M
		ii) Design a systolic array for the matrix-vector multiplication $y=A.x$ where A is a 4×4 matrix and x is a vector of size 4.	3	3	6M
		OR			
	b	i) A systolic array is used for a 1D FIR filter with 5 coefficients: $y[n]=h_0x[n]+h_1x[n-1]+h_2x[n-2]+h_3x[n-3]+h_4x[n-4]$. Design a systolic architecture for the given filter.	3	3	6M
		ii) For the above question, derive the data mapping schedule for input x[n] and coefficients h[k] across the array.	3	3	6M
4		Unit-IV			
	a	i)The Cook-Toom algorithm for fast convolution splits a 4-point convolution into smaller parts. Derive the steps to compute the convolution	3	4	6M

		of x[n] and h[n], where both sequences have 4 points: x = {x_0, x_1, x_2, x_3}and h = {h_0, h_1, h_2, h_3}. Also, show how the polynomial representation of the sequences is used to compute the result efficiently.			
		ii) Design a 3-point Cook-Toom convolution for upsampling a signal by a factor of 2. Compare the result with the direct convolution method and analyze the computational savings.	4	4	6M
		OR			
	b	i) Analyze the application of the Winograd algorithm in real-time signal processing systems.	4	4	6M
		ii)The Winograd F(4,3) algorithm is applied to compute the convolution of a 4-point input x[n] and a 3-point filter h[n]. Calculate the number of multiplications and additions required for this convolution.	3	4	6M
5		Unit-V			
	a	i) Consider a second-order lattice filter with the following parameters: • a_1=0.5, a_2=0.3 • b_1=0.7, b_2=0.4 • Input signal x[n] = {1,2,3,4}. Derive the difference equations for the lattice filter. Also, calculate the output y[n] for the given input signal x[n] using the lattice structure.	3	5	6M
		ii) Design a second-order lattice filter with the following specifications: • Passband frequency: 0.2 Hz • Stopband frequency: 0.5 Hz • Sample rate: 1 Hz • Desired attenuation: 40 dB in the stopband.	3	5	6M
		OR			
	b	i) Discuss various power reduction techniques in CMOS circuits.	2	5	6M
		ii) Derive an expression for the dynamic power consumption of a CMOS gate in terms of switching activity.	3	5	6M

KL: Blooms Taxonomy Knowledge Level CO: Course Outcome M:Marks

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NARASARAOPETA ENGINEERING COLLEGE
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R24

I M.TECH I Semester Regular Examinations, January-2025

Sub Code: R24MVL110 **CAD OF DIGITAL SYSTEM**

Time: 3 hours ECE (VLSI-ES) Max. Marks: 60

Note: Answer All **FIVE** Questions.

All Questions Carry Equal Marks (5 X 12M = 60M)

Q.No		Questions	KL	CO	M
1		Unit-I			
	a	i) Explain the various stages of the VLSI design flow, from system specification to layout generation.	2	1	6M
		ii) Analyze the design rules in the context of VLSI design and explain their importance.	4	1	6M
		OR			
	b	i) Discuss the impact of process variations on the design layout and the steps taken to mitigate these effects in modern VLSI design.	2	1	6M
		ii) What is the importance of technology scaling in VLSI fabrication? Analyze how it affects the design process, focusing on CMOS scaling and its limitations.	4	1	6M
2		Unit-II			
	a	i) Explain how graphs, trees, and linked lists are used in different stages of VLSI design	2	2	6M
		ii) Analyze how algorithms such as greedy algorithms and dynamic programming algorithms are applied in VLSI design tasks like placement and routing.	4	2	6M
		OR			
	b	i) Discuss in detail about Heuristic Algorithms.	2	2	6M
		ii)Analyze the computational complexity of simulated annealing algorithms.	4	2	6M
3		Unit-III			
	a	i) Discuss how graph partitioning can be applied to combinational optimization problems. Represent the problem as a graph G(V,E) where V represents tasks and E represents dependencies.	2	3	6M
		ii)Formulate a partitioning model for VLSI circuit design, where the objective is to minimize the wire length while partitioning the layout into sub-regions for efficient routing.	3	3	6M
		OR			
	b	i) Discuss the real-world applications of the Kernighan-Lin algorithm in areas such as VLSI design and circuit partitioning.	2	3	6M
		ii) Analyze the role of the gain function in the Kernighan-Lin algorithm. How does it drive the optimization process?	4	3	6M

4		Unit-IV			
	a	i) Explain the key principles of gate-level modeling in digital design. How does gate-level modeling differ from other levels of abstraction, such as behavioral and structural modeling?	2	4	6M
		ii) Describe the optimization techniques used in logic synthesis. Compare their effectiveness in reducing circuit complexity and improving performance.	4	4	6M
		OR			
	b	i) Discuss the significance of gate-level simulation in VLSI design and verification. What are its advantages, and in what scenarios is gate-level simulation preferred over higher-level simulations?	2	4	6M
		ii) Explain the role of hardware models in high-level synthesis. How do these models bridge the gap between high-level specifications and hardware implementations?	2	4	6M
5		Unit-V			
	a	i)Compare and Contrast various Multi Chip Modules.	2	5	6M
		ii) Analyze how hardware description languages like VHDL and Verilog are used in the design and implementation of Multi-Chip Modules (MCMs).	4	5	6M
		OR			
	b	i) Explain about MCM Maze Routing.	2	5	6M
		ii) Discuss in detail about Topological Routing.	2	5	6M

KL: Blooms Taxonomy Knowledge Level CO: Course Outcome M:Marks

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