NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

I M.TECH I Semester Regular Examinations, January-2025

R24

Sub Code: R24MCC101 **RESEARCH METHODOLOGY & IPR**
Time: 3 hours (MD,CSE, STRE, PID, DECS, VLSI&ES) Max. Marks: 60

Note: Answer All **FIVE** Questions.
All Questions Carry Equal Marks (5 X 12M = 60M)

Q.No		Questions	KL	CO	M
1		Unit-I			
	a	i) Explain Clearly the objectives of Research Problem	K2	1	6M
		ii) Interpret different sources of research problem by giving suitable examples	K2	1	6M
		OR			
	b	i) Explain clearly research design process and steps to be followed	K2	1	12M
2		Unit-II			
	a	i) How do you design a research problem? Give an example to illustrate your answer	K2	2	6M
		ii) Discuss various issues involved in selecting a research problem. Also elaborate important features of a good research design.	K2	2	6M
		OR			
	b	i) Differentiate between qualitative research and quantitative research	K2	2	12M
3		Unit-III			
	a	i) Explain the procedure to determine the size of sample and discuss on sampling size	K2	3	6M
		ii) Explain the Concepts of Statistical Population	K2	3	6M
		OR			
	b	Explain different types of sampling techniques	K2	3	12M
4		Unit-IV			
	a	i) Explain new developments in Intellectual Property Rights.	K2	4	6M
		ii) Define intellectual property in research. Explain different types of intellectual property	K2	4	6M
		OR			
	b	i) Contrast the purpose and functions of trademarks	K2	4	6M
		ii) Write notes on trade secrets, precautions and maintenance	K2	4	6M
5		Unit-V			
	a	i) Exemplify the basic criteria of patentability of industrial designs	K2	5	6M
		ii) Explain the fundamentals of copyright laws	K2	5	6M
		OR			
	b	i) Describe briefly how the online patent data is organized	K3	5	6M
		ii) Describe the structure and content of a patent document in general.	K3	5	6M

KL: Blooms Taxonomy Knowledge Level CO: Course Outcome M: Marks

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NARASARAOPETA ENGINEERING COLLEGE
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I M. Tech I Semester Regular Examinations, January-2025

Sub Code: R24MNC102 **DISASTER MANAGEMENT**

Time: 3 hours (STRE, P&ID, MD,DECS,VLSI&ES and CSE) Max. Marks: 60

Note: Answer All **FIVE** Questions.

All Questions Carry Equal Marks (5 X 12 = 60M)

Q.No		Questions	KL	CO	M
1		Unit-I			
	a	i) Describe types of disasters with examples.	K2&K3	C01	6M
		ii)) Explain About The Disaster Management Cycle	K2&K3	C01	6M
		OR			
	b	i) Explain how the Richter scale is used to measure the magnitude of an earthquake	K2&K3	C01	6M
		ii) Discuss various types of natural disasters in India and highlight their effects	K2&K3	C01	6M
2		Unit-II			
	a	Explain The causes of Floods and the effects of Floods in detail. Give one Case Study of The Floods.	K2&K3	C02	12M
		OR			
	b	Explain The causes of earthquakes and effects of earthquakes in detail. Give one Case Study of The earthquake.	K2&K3	C02	12M
3		Unit-III			
	a	i) Explain the Earthquake zones of India	K2&K3	C03	6M
		ii) explain assessing risk and vulnerability	K2&K3	C03	6M
		OR			
	b	What is drought? Explain the types of droughts. Explain drought mitigation with an integration of technology and people.	K2&K3	C03	12M
4		Unit-IV			
	a	i) what are the multimedia technologies of disaster risk management in remote sensing	K2&K3	C04	12M
		OR			
	b	i) what are the forewarning levels of disaster management	K2&K3	C04	6M
		ii) Explain About The Mass Media and disaster Management?	K2&K3	C04	6M
5		Unit-V			
	a	i) what are the disaster management acts and policies in India	K2&K3	C05	6M
		ii) What are the steps for formulating a disaster risk reduction plan?	K2&K3	C05	6M
		OR			
		What are favourable conditions for cyclone formation? How do you estimate risk from cyclonic conditions and safety precautions to save lives?	K2&K3	C05	12M

NARASARAOPETA ENGINEERING COLLEGE
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I M.TECH I Semester Regular Examinations, January-2025

Sub Code: R24MDE102 **DIGITAL SYSTEM DESIGN**

Time: 3 hours (DECS) Max. Marks: 60

Note: Answer All **FIVE** Questions. All Questions Carry Equal Marks (5 X 12M = 60M)

Q.No		Questions	KL	CO	M
1		Unit-I			
	a	i) Explain the tabular method for minimizing switching functions with a step-by-step procedure.	K2	1	6M
		ii) Minimize the given Boolean function using the K-map method:f(A,B,C,D)=$\prod$M(1,3,5,7,9,11,13,15).	K3	1	6M
		OR			
	b	i) Compare and contrast the K-map and Quine-McCluskey algorithm for minimization of switching functions.	K3	1	6M
		ii) Simplify the Boolean function using a 4-variable K-map:f(A,B,C,D)= $\sum$ m(0,2,4,8,9,10,12,14. Draw the K-map and identify the minimized expression.	K3	1	6M
2		Unit-II			
	a	i) Describe the passport-checking process in Phase-II of the CAMP-I algorithm and its role in determining solution prime cubes (SPC).	K2	2	6M
		ii) Explain the concept of compatibility (CSC) and secondary state minimizations (SSMs) in the CAMP-I algorithm.	K2	2	6M
		OR			
	b	i) Discuss the steps involved in the CAMP-II algorithm for the determination of the solution cube and how cube-based operations are performed.	K2	2	6M
		ii) Discuss the determination of selected cubes in a switching function using cube-based algorithms.	K3	2	6M
3		Unit-III			
	a	i) Describe the architecture and block diagram of a Programmable Logic Array (PLA).	K3	3	6M
		ii) Explain the IISc algorithm for PLA minimization.	K2	3	6M
		OR			
	b	i) Discuss the advantages of using the IISc algorithm for PLA minimization over traditional methods such as K-map or QM algorithms.	K2	3	6M
		ii) Provide an overview of Programmable Logic Arrays (PLAs).	K3	3	6M
4		Unit-IV			
	a	i) Explain the concept of Algorithmic State Machine (ASM) charts and their significance in digital system design.	K2	4	6M
		ii) Explain how an ASM chart is realized in a digital circuit.	K2	4	6M
		OR			
	b	i) Describe the control implementation in digital systems using ASM charts.	K2	4	6M
		ii) Discuss the various digital system design approaches using Field-Programmable Gate Arrays (FPGAs).	K2	4	6M
5		Unit-V			
	a	i) Discuss the steps involved in the fault diagnosis and testing process for combinational circuits.	K2	5	6M
		ii) Explain the concept of Design for Testability (DFT) schemes. How do these schemes help in fault diagnosis?	K2	5	6M

		OR			
	b	i) Discuss the principles of Built-In-Self-Test (BIST) in combinational circuits.	K2	5	6M
		ii) Using the Kohavi algorithm, determine whether a fault is detectable in a given circuit. Explain each step of the process.	K3	5	6M

KL: Blooms Taxonomy Knowledge Level CO: Course Outcome M:Marks

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NARASARAOPETA ENGINEERING COLLEGE
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I M.TECH I Semester Regular Examinations, January-2025

R24

Sub Code: R24MDE103 **DIGITAL DATA COMMUNICATIONS**

Time: 3 hours ECE (DECS) Max. Marks: 60

Note: Answer All **FIVE** Questions. All Questions Carry Equal Marks (5 X 12M = 60M)

Q.No			Questions	KL	CO	M
1			Unit-I			
	a	i)	Sketch the QPSK waveform for the sequence 1101010010, assuming the carrier frequency equal to bit rate. What is the difference between BPSK and QPSK?	3	1	6M
		ii)	Draw the block diagram, Explain the base band decoder used to recover the signal in a BPSK system i.e, DPSK decoder?	3	1	6M
			OR			
	b	i)	Determine the bandwidth required for M-ary FSK system. Draw the geometrical representation of M-ary FSK signals and find out the distance between the signals.	3	1	6M
		ii)	Draw and explain the signal space representation of the QPSK. List the advantages of it.	2	1	6M
2			Unit-II			
	a	i)	Explain the role of a sender, receiver, and transmission medium in a data communication system.	2	2	6M
		ii)	What are the functions of a DTE-DCE? Explain with one example.	2	2	6M
			OR			
	b	i)	How does a modem convert digital signals into analog signals and vice versa?	3	2	6M
		ii)	Explain how I2C facilitates communication between microcontrollers and peripheral devices.	2	2	6M
3			Unit-III			
	a	i)	How does the Longitudinal Redundancy Check (LRC) differ from VRC?		3	6M
		ii)	What is CRC? If the generating polynomial for CRC code is $x^4 + x^3 + 1$ and message word is 11110000, determine check bits and codeword.	3	3	6M
			OR			
			A memory less source emits six messages with probabilities 0.3, 0.25, 0.15, 0.12, 0.1 and 0.08. Find the Huffman code. Determine its average word length, the efficiency and the redundancy.	3	3	12M
4			Unit-IV			
	a	i)	Explain the function of error control in data link layer.	2	4	6M
		ii)	Discuss about bit-oriented protocol with diagram.	2	4	6M
			OR			
	b	i)	Explain the difference between stop-and-wait flow control and sliding window flow control.	2	4	6M
		ii)	What is meant by polling? Explain in brief.	2	4	6M
5			Unit-V			
	a	i)	Discuss about IEEE 802.6 standard in MANs.	2	5	6M
		ii)	Describe about the Technological features of CDMA and its limitations.	2	5	6M
			OR			
	b	i)	Compare and contrast circuit switching and packet switching techniques	4	5	6M
		ii)	What is Aloha and explain about carrier sense multiple access.	2	5	6M

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I M.TECH I Semester Regular Examinations, January-2025

Sub Code: R24MDE105 **VLSI TECHNOLOGY & DESIGN**

Time: 3 hours ECE (DECS) Max. Marks: 60

Note: Answer All **FIVE** Questions.

All Questions Carry Equal Marks (5 X 12M = 60M)

Q.No		Questions	KL	CO	M
1		Unit-I			
	a	i) Explain the significance of VLSI technology in modern electronic systems. Discuss its major applications.	L2	1	6M
		ii) What are the different stages involved in wafer fabrication? Explain each stage briefly.	L1	1	6M
		OR			
	b	i) Describe the placement and routing stages in the physical design flow and their significance.	L2	1	6M
		ii) Discuss the critical design issues in VLSI related to power, performance, and area.	L2	1	6M
2		Unit-II			
	a	i) Describe the steps involved in the fabrication process of pMOS technology and highlight its applications.	L2	2	6M
		ii) What are lambda-based design rules, and why are they important in CMOS circuit design?	L1	2	6M
		OR			
	b	i) Compare pMOS, nMOS, CMOS, and Bi-CMOS technologies based on power consumption, performance, and fabrication cost.	L3	2	6M
		ii) Explain the importance of communication interfaces in VLSI systems and describe their basic design principles.	L2	2	6M
3		Unit-III			
	a	i) Discuss the importance of technology options VLSI Design process.	L2	3	6M
		ii) Explain about the power calculations in VLSI Design process.	L2	3	6M
		OR			
	b	i) What is the importance of mixed signal design in VLSI Design process.	L1	3	6M
		ii) Explain the solutions for VLSI Design Issues.	L2	3	6M
4		Unit-IV			
	a	i) Explain the concept of Basic electrical properties of MOS and BiCMOS circuits.	L2	4	6M
		ii) Discuss about the MOS and BiCMOS circuit design processes.	L2	4	6M
		OR			
	b	i) Explain the procedure for Scalable CMOS Design Rules.	L2	4	6M
		ii) Discuss the scaling of MOS circuits-qualitative and quantitative analysis.	L2	4	6M
5		Unit-V			
	a	i) Explain about the concept of some clocked sequential circuits.	L2	5	6M
		ii) Describe the procedure for Floor planning methods.	L3	5	6M

		OR			
	b	i) Explain the design of an ALU subsystem.	L2	5	6M
		ii) What are the design methodologies in chip design and explain.	L1	5	6M

KL: Blooms Taxonomy Knowledge Level CO: Course Outcome M:Marks

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NARASARAOPETA ENGINEERING COLLEGE
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I M.TECH I Semester Regular Examinations,January-2025

R24

Sub Code: R24MDE109 OPTICAL COMMUNICATION TECHNOLOGY

Time: 3 hours ECE (DECS) Max. Marks: 60

Note: Answer All FIVE Questions.

All Questions Carry Equal Marks (5 X 12M = 60M)

Q.No		Questions	KL	CO	M
1		Unit-I			
	a	i) Explain various approaches related to propagation of light in OFC	2	1	6M
		ii) What is polarization of light, and how can light be polarized?	2	1	6M
		OR			
	b	i) Explain various Scattering techniques in OFC	2	1	6M
		ii) Explain about Four Wave Mixing and Principle of Solitons.	2	1	6M
2		Unit-II			
	a	i) What are the functions of optical switches? Explain?	3	2	6M
		ii) Explain the principle of operation of optical amplifier.	1	2	6M
		OR			
	b	i)Explain about High Channel Count Multiplexer Architectures	2	2	6M
		ii) Explain the principle of operation of a Circulator	2	2	6M
3		Unit-III			
	a	i) Explain subcarrier modulation and multiplexing	3	3	6M
		ii) Explain the Duobinary optical modulation scheme with necessary diagrams.	3	3	6M
		OR			
	b	i) Explain in detail about optical modulation schemes	1	3	12M
4		Unit-IV			
	a	i)Explain about Ideal and Practical Receivers for Demodulation	1	4	6M
		ii) What are the different types of error detection codes in optical system? Explain.	2	4	6M
		OR			
	b	i)Explain about Power Penalty in Transmitter and Receiver	2	4	6M
		ii) Find the expression for Bit Error Rate (BER) IN Ideal receivers and also calculate the BER in Practical receiver with different noise impairments	4	4	6M
5		Unit-V			
	a	i) Explain about WDM system and its principle with neat diagram?	2	5	6M
		ii) Explain the wavelength stabilization against Temperature variations in an Optical Networks?	2	5	6M
		OR			
	b	Explain Overall System Design considerations i) Fiber Dispersion ii)Modulation iii) Non-Linear Effects iv)Wavelengths	3	5	12M

KL: Blooms Taxonomy Knowledge Level CO: Course Outcome M:Marks

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